IPSmart

12-Bit 320MSPS IQ DAC in SMIC 40nm L

IPS_S40_DAC12X2_320M

FEATURES

- **Dual 12-bit DAC, up to 320 MSPS**
- **Dual 3.3 V / 1.15 V Supply**
- **Low Power Consumption**
  50mW @ 320 MSPS
- **Superior Dynamic Range**
  71dBc SFDR @ f_{out} = 40 MHz
- **IFS = 6mA with programmability**
- **Output voltage: 1Vppd**
- **Programmable termination resistor**
- **Ultra Small Core Area: 460um X 460um= 0.21 mm^2**
- **SMIC 40LP 1P6M**

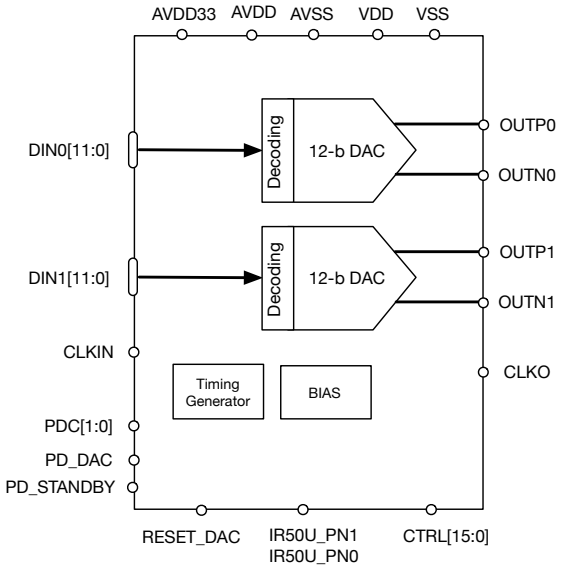


Figure 1. BLOCK DIAGRAM

APPLICATIONS

- **WiFi / LTE / WiMax**
- **Wireless MIMO**
- **Digital Video**
- **Communication Transmit**

GENERAL DESCRIPTION

S40L_DAC12X2_320M is compact and low power 12-bit digital-to-analog converter silicon IP in SMIC 40nm LP process. It features two channel current steering DAC.

This IQ DAC IP is optimized for low power and small area. At 320 MHz conversation rate, it only consumes 56mW and occupies silicon area of 0.21 mm^2.

TABLE OF CONTENTS

REVISION HISTORY

Revision	Date	Description
1.0	12/21/2017	Initial revision

DC SPECIFICATIONS

T_j = 25°C, AVDD33 = 3.3 V, DVDD = 1.15V, CLKIN= 320 MHz , unless otherwise noted.

Table 1. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		12		bits
Monotonicity		B		Guaranteed		
Differential Nonlinearity (DNL)		B		±0.5	±1	LSB
Integral Nonlinearity (INL)		B		±1	±3	LSB
Full-scale Output Current		B		6		mA
Output Common Mode Voltage		B		0.5		V
Output Load Capacitance		B			0.5	pF
Full-scale Output Differential Voltage		B		1.0		Vppd
Gain Matching between IQ channels		B		±0.5		% FS
Offset Error		B			±0.1	% FS
Operating Junction Temperature (Tj)		B(1)	-40		125	°C
Analog Supply High Voltage AVDD33		B	3.0	3.3	3.6	V
Analog Supply Core Voltage AVDD		B	1.09	1.15	1.21	V
Digital Supply Voltage VDD		B	0.99	1.1	1.21	V
AVDD33 Supply Current		B		15	20	mA
AVDD Supply Current		B		6	12	mA
Power Dissipation		B		56	86	mW
Power Down Current		B		15	90	uA

(1) Measurement temperature 0~85C

AC SPECIFICATIONS

T_j = 25˚C, AVDD33 = 3.3 V, DVDD = 1.15V, CLKIN= 320 MHz, unless otherwise noted.

Table 2. AC Performance

Parameter	Test conditions	Test	Min	Typ	Max	Unit
Maximum Conversion Rate		B	320			MHz
Signal-to-Noise Ratio (SNR)	f_{out} = 40 MHz	B	64	67		dBFS
Spurious Free Dynamic Range (SFDR)	f_{out} = 40 MHz	B	68	71		dBc
Total Harmonic Distortion (THD)	f_{out} = 40 MHz	B	-67	-69		dBc
Signal-toNoise Distortion (SNDR)	f_{out} = 40 MHz	B	62	65		dBFS
ENOB		B	10	10.5		Bits
Channel Isolation		B	70			dBc
Wake-up Time from Standby mode		B		100		ns
Start-up Time from Power Down (reference is disabled)		B		1		us

Test Categories

A. Preliminary target specification.

B. Simulation of the design over process, voltage, and temperature (PVT)[(1)].

C. Measurements on a set of samples at typical process over voltage and temperature.

D. Measurements on a set of samples at process corners over voltage and temperature.

DIGITAL SPECIFICATIONS

Table 3. Switching Specifications

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Clock Duty Cycles		B	48		52	%
Aperture Delay		B		0.1		ns
Aperture Jitter		B		<3		ps rms

OPERATION MODES

Table 4. Mode of Operation

Mode	Description	Control bits	Recover to normal operation time
Normal operation	All functional blocks are enabled	PD_STANDBY= PD_DAC= low	N/A
Standby	Clock function is disabled	PD_STANDBY= high	100 ns (wake-up time)
Power down	All functional blocks are disabled	PD_DAC= high	1 us (power-up time)

PIN DESCRIPTION

Table 5. Pin Function Descriptions (total 20 pins)

Index	Pin Name	I/O	Description
1	AVDD33	AP	Analog power supply 3.3V
2	AVDD	AP	Analog power supply 1.15V
3	VDD	DP	Digital power supply 1.1V
4	AVSS	AG	Analog ground for AVDD33 and AVDD
5	VSS	DG	Digital ground for VDD
6	DIN0[11:0], DIN1[11:0]	DI	Digital inputs
7	CLKIN	DI	Clock input
8	IR50U_PN1, IR50U_PN0	AI	50uA reference current input PMOS sent, NMOS received
9	OUTP0/OUTN0	AO	Channel 0 differential outputs (Channel I)
10	OUTP1/OUTN1	AO	Channel 1 differential outputs (Channel Q)
11	PDC[1:0]	DI	DAC channel power down control (logic 1 → power down)
12	PD_STANDBY	DI	DAC standby mode, clock is disabled
13	PD_DAC	DI	DAC power down mode, all blocks are disabled
14	CTRL[15:0]	DI	Programmable control bits
15	CLKO	DO	DAC output clock
16	RESET_DAC	DI	Clock divider RESET signal

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

OUTPUT LOAD MODEL

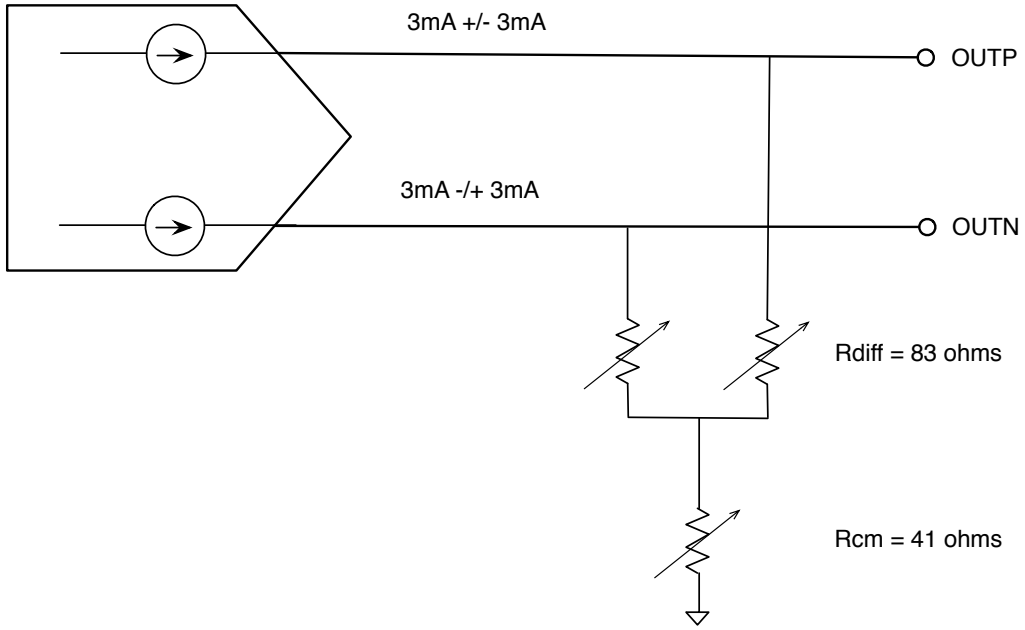


Fig. 2. DAC LOAD MODEL

TIMING DIAGRAM

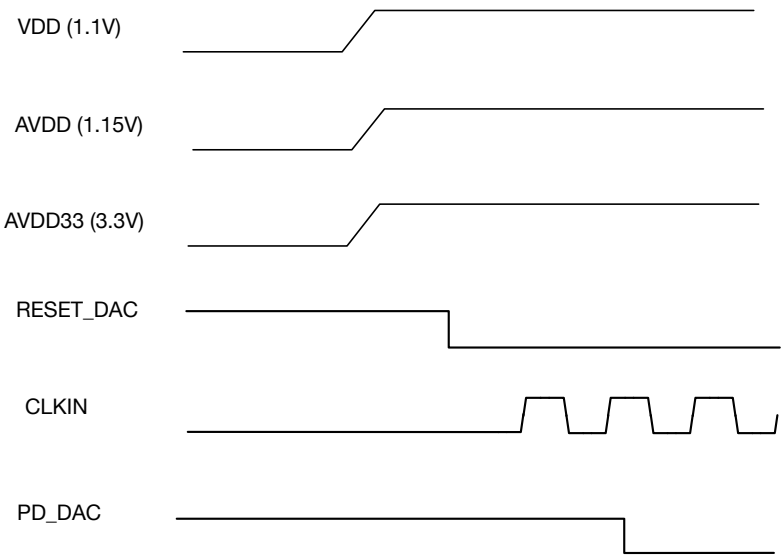
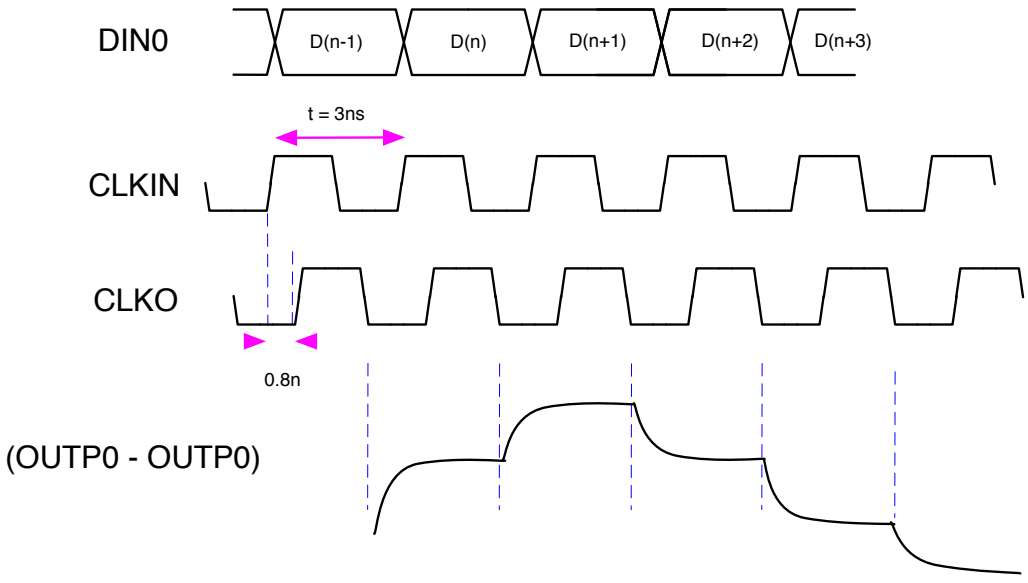


Fig. 3. DAC Power up Sequence



Note: DAC outputs change at the falling edge of CLKO

Fig. 4. DAC Normal Operation Timing Diagram

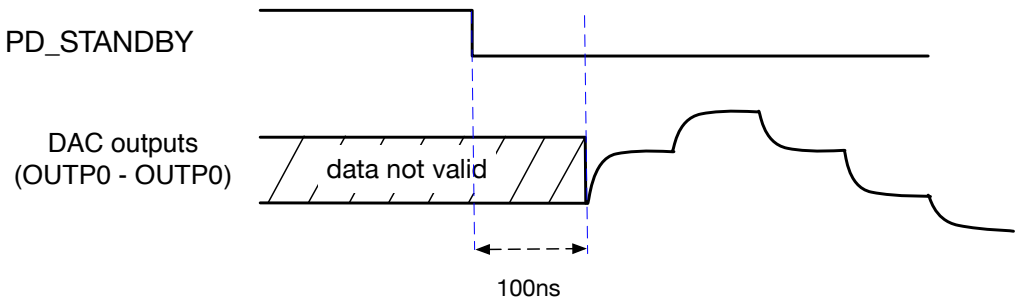


Fig. 5. Timing Diagram of Wake-Up from standby mode

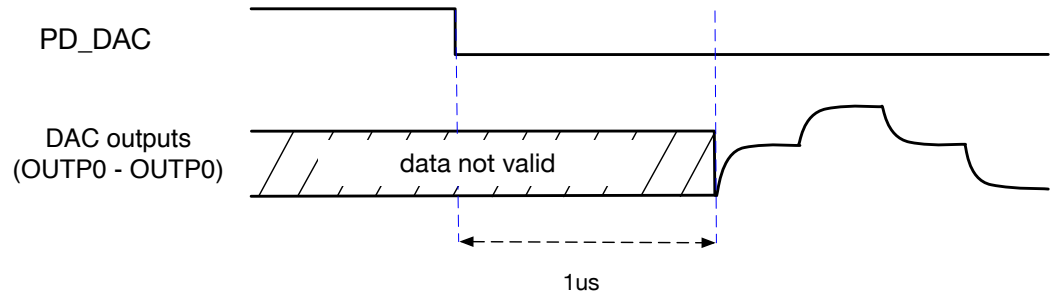


Fig. 6. Timing Diagram of Power-Up from power down mode

CONTROL BITS DESCRIPTION

Table 6. Full Scale Current Control

CTRL[1:0]	Description
1 1	6.5 mA
1 0 (default)	6.0 mA
0 1	5.5 mA
0 0	5.0 mA

Table 7. Loading Control

CTRL[3:2]	Description
1 1	90 ohms
1 0 (default)	83 ohms
0 1	77 ohms
0 0	67 ohms

Table 8. Sampling Clock Edge Control

CTRL[5]	Description
1	Sample input data at the falling edge
0 (default)	Sample input data at the rising edge

Table 9. Conversion Rate Control

CTRL[7:6]	Description
1 1	DIV by 8
1 0	DIV by 4
0 1	DIV by 2
0 0 (default)	DIV by 1

Table 10. Input Data Sampling Delay Control

CTRL[9:8]	Description
1 1	100ps
1 0 (default)	200ps
0 1	300ps
0 0	400ps

Table 11. VCMO Voltage Control

CTRL[11:10]	Description
1 1	0.55
1 0 (default)	0.50
0 1	0.45
0 0	0.40

Table 12. Reserved Registers

CTRL[4]	Reserved
CTRL[15:12]	Reserved

Default CTRL[15:0] setting is 0000-1010-0000-1010 = 0A0Ah

PHYSICAL DESCRIPTION

IP Macro Layout

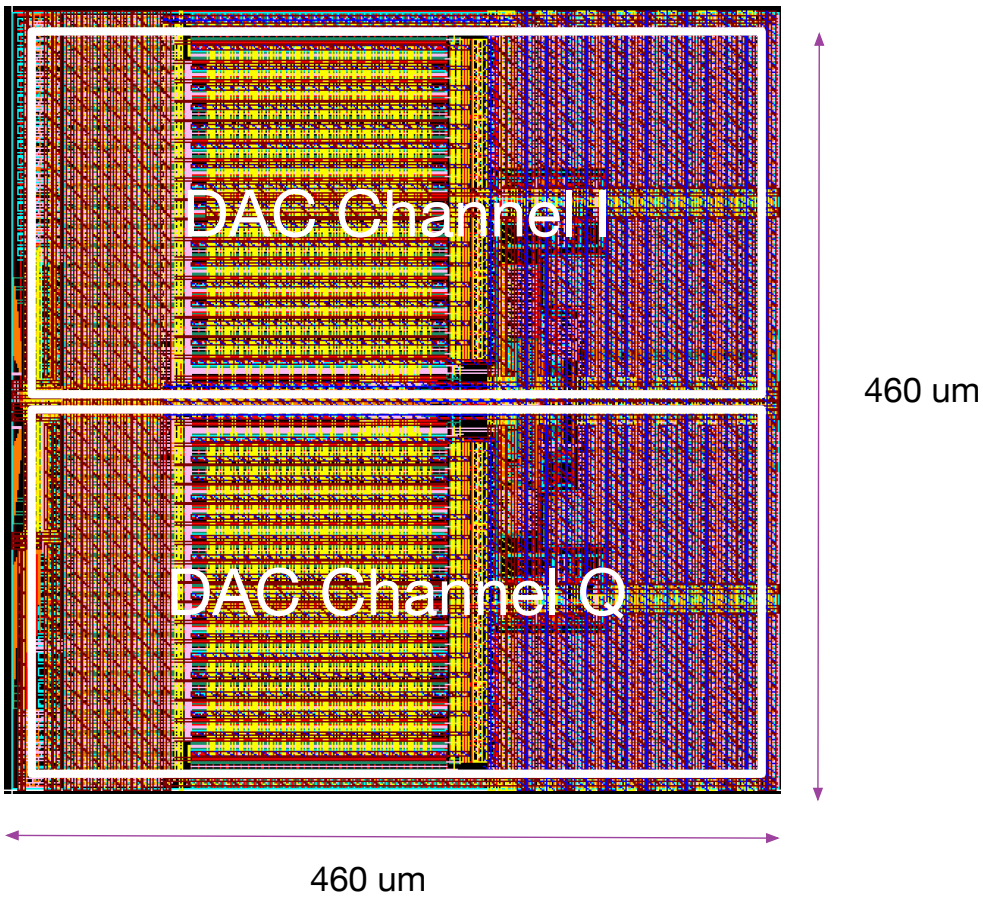


Fig. 7. IP macro layout.

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 12. Process Options

Item	Description
Process	SMIC 40nm LP
Metal Stack	1P5X
Resistor	P+ Poly, rnwod (N-Well under OD resistor)
Deep Nwell	No
IO PAD	-

DELIVERABLES

Complete design kit for fast and reliable integration of the IP is provided. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (System Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support