IPSmart

10-Bit 165 MSPS ADC in TSMC110nm

IPS_T110_ADC10_165M

FEATURES

- **Single Supply 1.2V**
- **165 MSPS Conversion Rate**
- **Current Consumption**
  36 mA @ 165 MSPS
- **Dynamic Performance @ 165MSPS**
  58 dBFS SNR
  -60 dBc THD
  62 dBc SFDR
  ENOB of 9.0
- **Programmable current setting**
- **Programmable ADC full scale**
- **Internal Bandgap reference**
- **Ultra Small Core Area: 0.21 mm^2**
- **TSMC 110/130nm 1P5M**

APPLICATIONS

- **Communication RX Channel**
- **RGB, HDTV, Video Application**
- **Digital Imaging**

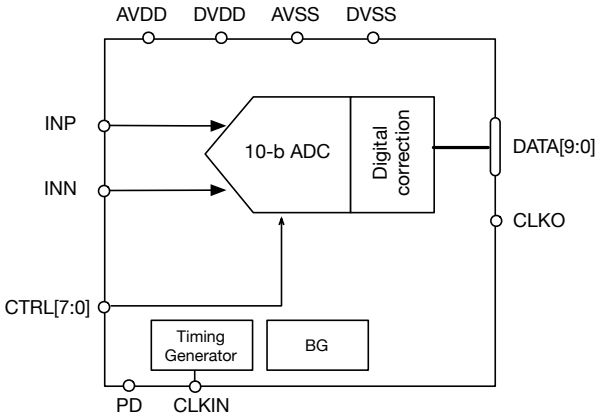

Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

IPS_T110_ADC10_165M is compact and low power 10-bit analog-to-digital converter silicon IP. This ADC uses 1.5b/stage pipelined architecture optimized for low power and small area. The ADC is designed for high dynamic performance for input frequencies up to Nyquist rate. This ADC consumes 36 mA at 165 MSPS operation and occupies silicon area of 0.21 mm^2. The ADC has high immunity to substrate noise and is ideal for SoC integration.

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REVISION HISTORY

Revision	Date	Description
1.0	5/1/2016	Initial revision

DC/AC SPECIFICATIONS

T_j = 25°C, AVDD = 1.2 V, f_{IN} = 10 MHz, f_S= 165 MHz, A_{IN} = -1 dBFS, unless otherwise noted.

Table 1. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		10		bits
Monotonicity		B		Guaranteed		
Differential Nonlinearity (DNL)		B		±0.6	±1	LSB
Integral Nonlinearity (INL)		B		±2	±3	LSB
Input Common-Mode Voltage		B		0.6		V
Input Differential Voltage Range		B		1.0		Vpp
Input Capacitance	single-ended	B		1.2		pF
Absolute Gain Accuracy		B		±1		% FS
Offset Error		B		±4		LSB
Operating Junction Temperature (Tj)		A(1)	-40		125	°C
Analog Supply Voltage AVDD		B	1.08	1.2	1.32	V
Digital Supply Voltage DVDD		B	1.08	1.2	1.32	V
AVDD Supply Current		B		35	44	mA
DVDD Supply Current		B		1	1	mA
Power Dissipation		B		43	54	mW
Power Down Current		B		8	26	uA

(1) Measurement temperature 0~85C

Table 2. AC Performance

Parameter	Test conditions	Test	Min	Typ	Max	Unit
Maximum Conversion Rate		B	165			MHz
Analog Input Bandwidth		B		200		MHz
Signal-to-Noise Ratio (SNR)		B	55	58		dBFS
Spurious Free Dynamic Range (SFDR)		B	58	62		dBc
Total Harmonic Distortion (THD)		B	-56	-60		dBc
Signal-toNoise Distortion (SNDR)		B	53	56		dBFS
ENOB		B	8.4	9.0		Bits

Test Categories

A. Preliminary target specification.
B. Simulation of the design over process, voltage, and temperature (PVT)[1].
C. Measurements on a set of samples at typical process over voltage and temperature.
D. Measurements on a set of samples at process corners over voltage and temperature.

DIGITAL SPECIFICATIONS

Table 3. Switching Specifications

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Clock Duty Cycles		A	45		55	%
Aperture Delay		A		0.5		ns
Aperture Jitter		A		<30		ps rms

PIN DESCRIPTION

Table 4. Pin Function Descriptions

Index	Pin Name	I/O	Description
1	AVDD	AP	Analog power supply 1.2V
2	DVDD	DP	Digital power supply 1.2V
3	AVSS	AG	Analog ground
4	DVSS	DG	Digital ground
5	INP/INN	AI	Analog differential inputs
6	CLKIN	DI	Input clock
7	PD	DI	ADC enable control input (logic 0 → power up, logic 1 → power down)
8	CLKO	DO	Output clock, can be used to sample DATA[9:0]
9	DATA[9:0]	DO	10-bit output data of ADC
10	CTRL[7:0]	DI	Programmable current setting and ADC full scale control bits

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

TIMING DIAGRAM

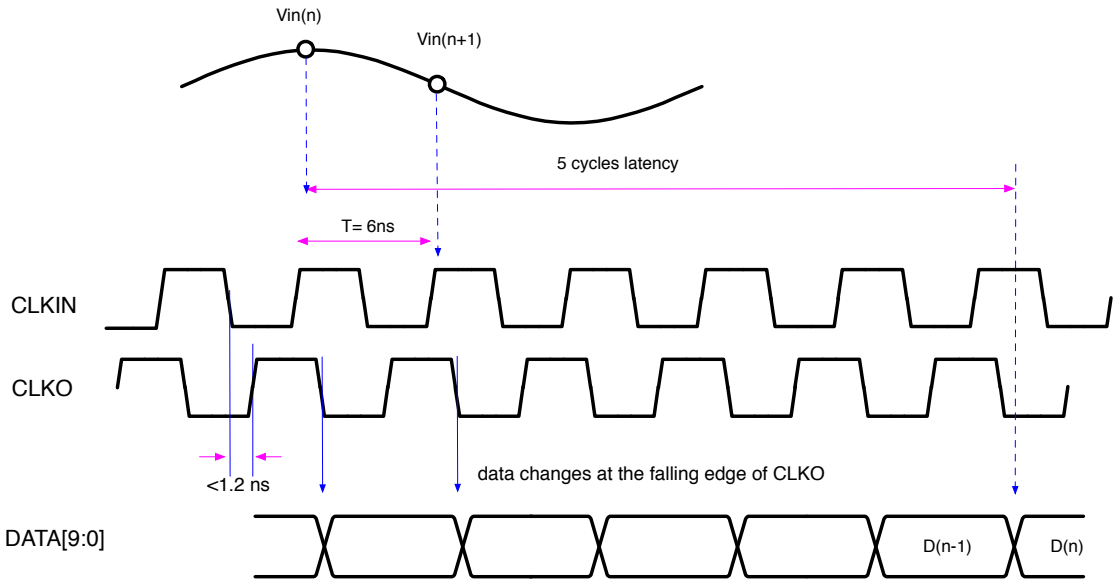

Figure 2. ADC Timing Diagram

CODE REPRESENTATION

Table 5. Code Description

Decimal	Hex	DATA[9:0] 2's complement
1FF	+511	01-1111-1111
000	0	00-0000-0000
201	-511	10-0000-0001

CONTROL BITS DESCRIPTION

Table 6. Bias Current Control

CTRL[1:0]	Description	Remarks
11	BIAS Current + 10%	
10	BIAS Current	default
01	BIAS Current -10%	
00	BIAS Current - 20%	

Table 7. OPAMP Bias Current Control

CTRL[3:2]	Description	Remarks
11	OPAMP BIAS + 17%	
10	OPAMP BIAS	default
01	OPAMP BIAS - 17%	For lower sampling rate
00	OPAMP BIAS - 34%	For lower sampling rate

Table 8. Reference Input

CTRL[4]	Description	Remarks
1	VDD referred bias	
0	Bandgap bias	default

Table 9. ADC Full Scale Control

CTRL[6:5]	Description	Remarks
11	1.04 V	
10	0.98 V	default
01	0.94 V	
00	0.89 V	

Table 10. ATST Monitor Voltage Control

CTRL[7]	ATST0	ATST1
1	BIASP (0.8V)	BIASN (0.4V)
0	REFP (0.9V)	VCM (0.6V)

PHYSICAL DESCRIPTION

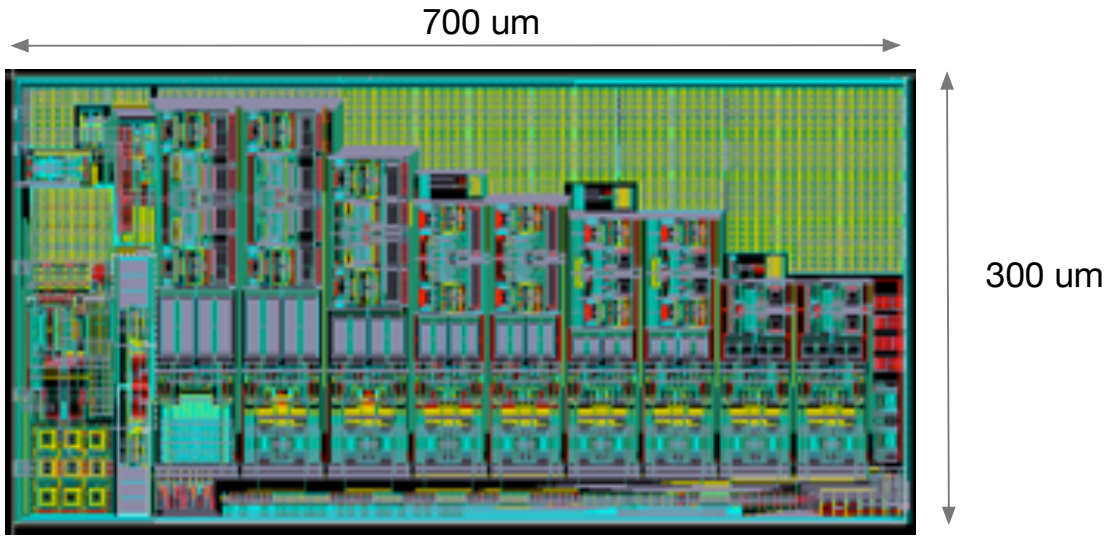

Fig. 4. IP macro layout.

DEFINITION OF SPECIFICATIONS

Offset Error

For a given gain setting, an AFE/ADC ideally produces mid-code at the output when differential input is zero. The input voltage that produces mid-code at the output is defined as the offset error.

Gain Error

AFE/ADC gain error is defined as the difference between ideal and actual full-scale values on input-output characteristics for a given gain setting when the offset error has been reduced to zero.

Integral Non Linearity (INL)

Integral non linearity of AFE/ADC transfer characteristics is defined as the deviation of the actual transfer characteristics from the ideal characteristic for a given gain setting after both offset and gain errors have been compensated. Ideal characteristic is defined as the straight line that is the best-fit of converter's transfer response.

Differential Non Linearity (DNL)

Differential non linearity of AFE/ADC transfer characteristics is defined as the deviation of analog step size from ideal step size of one LSB for a given gain setting.

ADC Latency

AFE/ADC latency (t_{pd}) is defined as the number of clock cycles between sampling edge of the clock and the clock edge at which corresponding digital outputs become available.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio is defined as the ratio of signal power to total power of all spectral components excluding DC and first eight harmonics.

Signal-to-Noise and Distortion Ratio (SNDR)

Signal-to-noise and distortion ratio is defined as the ratio of signal power to total power of all spectral components excluding DC.

Effective Number of Bits (ENOB)

Effective number of bits represents the effective resolution of the AFE. ENOB is calculated from SNDR as follows:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

Total harmonic distortion is defined as the ratio of total power of first eight harmonics to the power of fundamental signal.

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range is the difference of amplitudes in dB between signal and the highest spectral component. The highest spectral component may or may not be a harmonic.

EFFECTS OF CLOCK JITTER

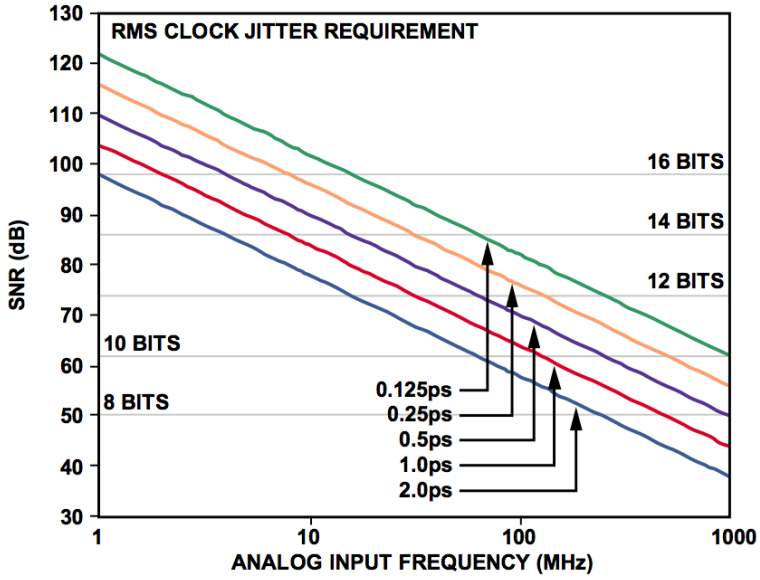

Fig. 5 Ideal SNR vs. Input Frequency and Jitter

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 11. Process Options

Item	Description
Process	TSMC 110nm/130nm
Metal Stack	1P5M
Capacitor	MOMCAP
Resistor	RPPOLY
Deep Nwell	No
IO PAD	-

DELIVERABLES

IPSmart provides a complete design kit for fast and reliable integration of the IP into customer's design flow. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support