IPSmart

12-Bit 320MSPS IQ DAC in IBM SOI 180nm

IPS_I180_DAC12X2_320M

FEATURES

- **12bit, up to 320 MSPS**
- **Dual 2.5 V / 1.5 V Supply**
- **Low Power Consumption**
  63mW @ 320 MSPS
- **Dynamic Range**
  72dBc SFDR @ f_{out} = 20 MHz
- **IFS = 6mA with programmability**
- **Output voltage: 1Vppd**
- **Programmable loading**
- **Ultra Small Core Area: 410um X 620um= 0.25 mm^2**
- **IBM 180nm SOI 1P4M**

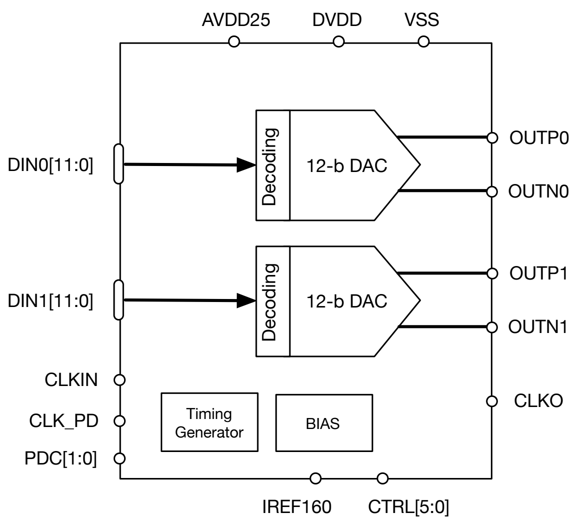

Figure 1. BLOCK DIAGRAM

APPLICATIONS

- **WiFi / LTE / WiMax**
- **Wireless MIMO**
- **Digital Video**
- **Communication Transmit**

GENERAL DESCRIPTION

IPS_I180_DAC12X2_320M is compact and low power 12-bit digital-to-analog converter silicon IP in IBM 180nm SOI process. It features two channel current steering DAC.

This IQ DAC IP is optimized for low power and small area. At 320 MHz conversation rate, it only consumes 63mW and occupies silicon area of 0.25 mm^2.

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REVISION HISTORY

Revision	Date	Description
0.1	7/16/2016	Initial revision

DC SPECIFICATIONS

T_j = 25˚C, AVDD25 = 2.5 V, VDD = 1.5V, CLKIN= 320 MHz , unless otherwise noted.

Table 1. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		12		bits
Monotonicity		B		Guaranteed		
Differential Nonlinearity (DNL)		B		±0.5	±1	LSB
Integral Nonlinearity (INL)		B		±1	±3	LSB
Full-scale Output Current		B		6		mA
Output Common Mode Voltage		B		0.25		V
Output Load Capacitance		B			0.5	pF
Full-scale Output Differential Voltage		B		1.0		Vppd
Gain Matching between 2 channels				±0.5		% FS
Offset Error		B			±0.1	% FS
Operating Junction Temperature (Tj)		B[1]	-40		125	˚C
Analog Supply Voltage AVDD25		B	2.25	2.5	2.75	V
Digital Supply Voltage DVDD		B	1.35	1.5	1.65	V
AVDD25 Supply Current		B		15	17	mA
DVDD Supply Current		B		17	19	mA
Power Dissipation		B		63	78	mW
Power Down Current		B		30		uA

[1] Measurement temperature 0~85C

AC SPECIFICATIONS

T_j = 25˚C, AVDD25 = 2.5 V, VDD = 1.5V, CLKIN= 320 MHz, unless otherwise noted.

Table 2. AC Performance

Parameter	Test conditions	Test	Min	Typ	Max	Unit
Maximum Conversion Rate		B	320			MHz
Analog Output Bandwidth				100		MHz
Signal-to-Noise Ratio (SNR)	f_{out} = 20 MHz	B	68	70		dBFS
Spurious Free Dynamic Range (SFDR)	f_{out} = 20 MHz	B	69	72		dBc
Total Harmonic Distortion (THD)	f_{out} = 20 MHz	B	-66	-69		dBc
Signal-toNoise Distortion (SNDR)	f_{out} = 20 MHz	B	64	67		dBFS
ENOB		B	10.3	10.7		Bits
Channel Isolation		B	70			dBc
Start-up Time from Power Down		B		0.2		us

Test Categories

A. Preliminary target specification.

B. Simulation of the design over process, voltage, and temperature (PVT)(1).

C. Measurements on a set of samples at typical process over voltage and temperature.

D. Measurements on a set of samples at process corners over voltage and temperature.

DIGITAL SPECIFICATIONS

Table 3. Switching Specifications

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Clock Duty Cycles		B	45		55	%
Aperture Delay		B		0.1		ns
Aperture Jitter		B		<30		ps rms

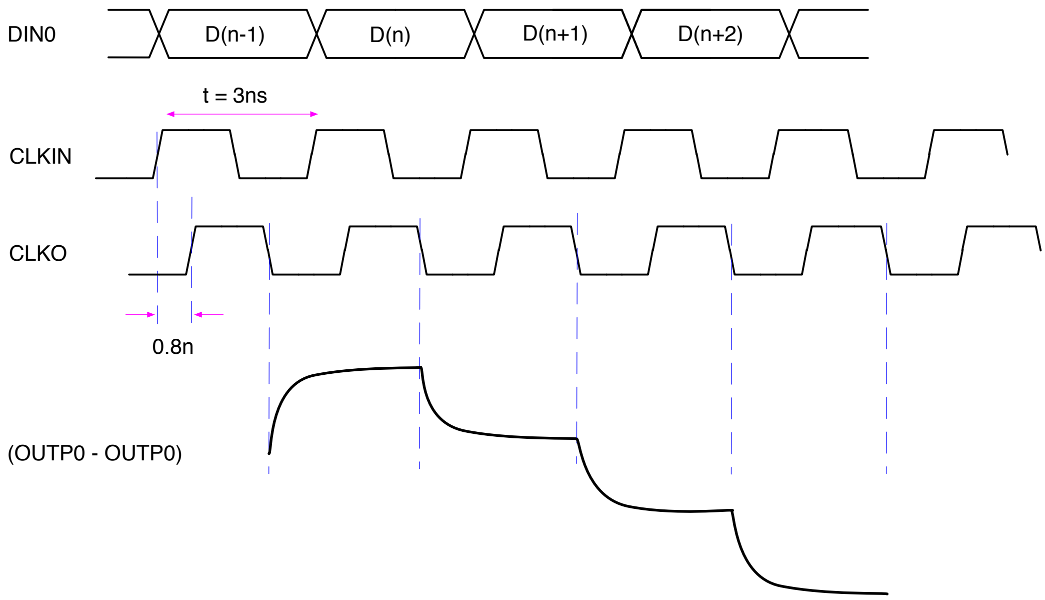
PIN DESCRIPTION

Table 4. Pin Function Descriptions

Index	Pin Name	I/O	Description
1	AVDD25	AP	Analog power supply 2.5V
2	DVDD	DP	Digital power supply 1.5V
3	VSS	DG	DAC ground
4	DI0[11:0], DI1[11:0]	DI	Digital inputs
5	CLKIN	DI	Clock input
6	IREF160	AI	Reference current input PMOS sent, NMOS received
7	OUTP0/OUTN0	AO	Channel 0 differential outputs (Channel I)
8	OUTP1/OUTN1	AO	Channel 1 differential outputs (Channel Q)
9	PDC[1:0]	DI	DAC channel power down control (logic 1 → power down)
10	CLK_PD	DI	CLK power down control (logic 1 → power down)
11	CTRL[5:0]	DI	Programmable control bits
12	CLKO	DI	DAC output clock

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

TIMING DIAGRAM



Note: DAC outputs change at the falling edge of CLKO

Fig. 2. DAC Timing Diagram

CODE REPRESENTATION

Table 5. Binary Code Representation

D[11:0] 2's Complement	Hex	Decimal
0111-1111-1111	7FF	+8191
0000-0000-0000	000	0
1000-0000-0000	100	-8191

CONTROL BITS DESCRIPTION

Table 6. Full Scale Current Control

CTRL[1:0]	Description
1 1	6.5 mA
1 0 (default)	6.0 mA
0 1	5.5 mA
0 0	5.0 mA

Table 7. Loading Control

CTRL[3:2]	Description
1 1	90 ohms
1 0 (default)	83 ohms
0 1	77 ohms
0 0	67 ohms

Table 8. Demux delay Control

CTRL[4]	Description
1	1ns
0 (default)	2ns

Note: This is to adjust the setup/hold time of the flops in demux

Table 9. Clock Inverting Control

CTRL[5]	Description
1	Clock inverted, I/Q channel swap
0 (default)	Clock not inverted

PHYSICAL DESCRIPTION

IP Macro Layout

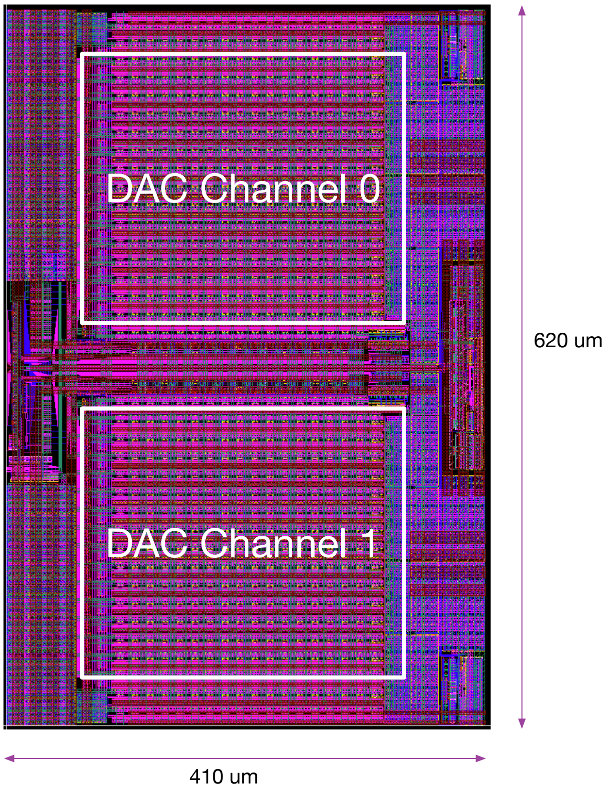


Fig. 3. IP macro layout.

DEFINITION OF SPECIFICATIONS

Offset Error

For a given gain setting, an AFE/ADC ideally produces mid-code at the output when differential input is zero. The input voltage that produces mid-code at the output is defined as the offset error.

Gain Error

AFE/ADC gain error is defined as the difference between ideal and actual full-scale values on input-output characteristics for a given gain setting when the offset error has been reduced to zero.

Integral Non Linearity (INL)

Integral non linearity of AFE/ADC transfer characteristics is defined as the deviation of the actual transfer characteristics from the ideal characteristic for a given gain setting after both offset and gain errors have been compensated. Ideal characteristic is defined as the straight line that is the best-fit of converter's transfer response.

Differential Non Linearity (DNL)

Differential non linearity of AFE/ADC transfer characteristics is defined as the deviation of analog step size from ideal step size of one LSB for a given gain setting.

ADC Latency

AFE/ADC latency (t_{pd}) is defined as the number of clock cycles between sampling edge of the clock and the clock edge at which corresponding digital outputs become available.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio is defined as the ratio of signal power to total power of all spectral components excluding DC and first eight harmonics.

Signal-to-Noise and Distortion Ratio (SNDR)

Signal-to-noise and distortion ratio is defined as the ratio of signal power to total power of all spectral components excluding DC.

Effective Number of Bits (ENOB)

Effective number of bits represents the effective resolution of the AFE. ENOB is calculated from SNDR as follows:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

Total harmonic distortion is defined as the ratio of total power of first eight harmonics to the power of fundamental signal.

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range is the difference of amplitudes in dB between signal and the highest spectral component. The highest spectral component may or may not be a harmonic.

EFFECTS OF CLOCK JITTER

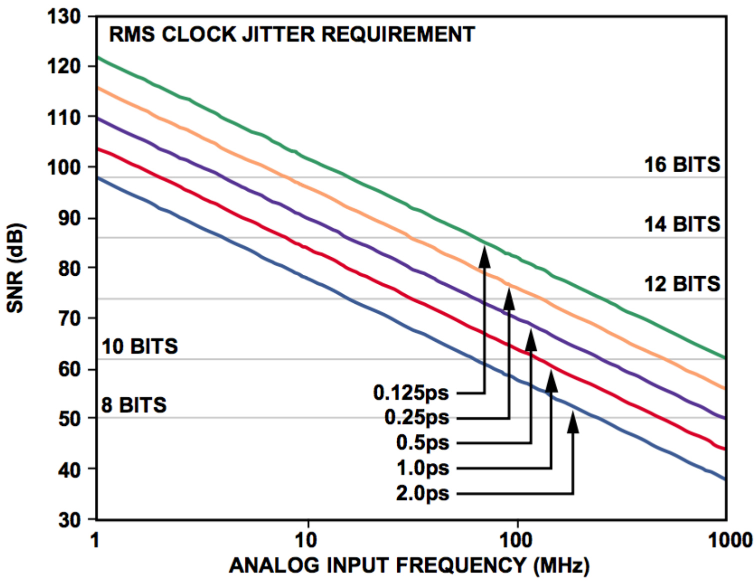


Fig. 4 Ideal SNR vs. Input Frequency and Jitter

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 10. Process Options

Item	Description
Process	IBM 180nm SOI
Metal Stack	4M
Resistor	OPPPCRES, OPRRPRES
Deep Nwell	No
IO PAD	-

DELIVERABLES

IPSmart provides a complete design kit for fast and reliable integration of the IP into customer's design flow. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support