IPSmart

14-Bit 1MSPS DAC in GSMC110nm

IPS_GS110_DAC14_1M

FEATURES

- **Wide Supply Range 1.7 V to 5.6V**
- **14bit, up to 1 MSPS Conversion Rate**
- **Low Power Consumption**
  680 uA @ 1 MSPS
- **Wide output range: 0.1 to 0.9 of Supply voltage**
- **Drive 15K/50pF loading**
- **Ultra Small Core Area: 250um X 300um= 0.075 mm^2**
- **GSMC 110nm 1P5M**

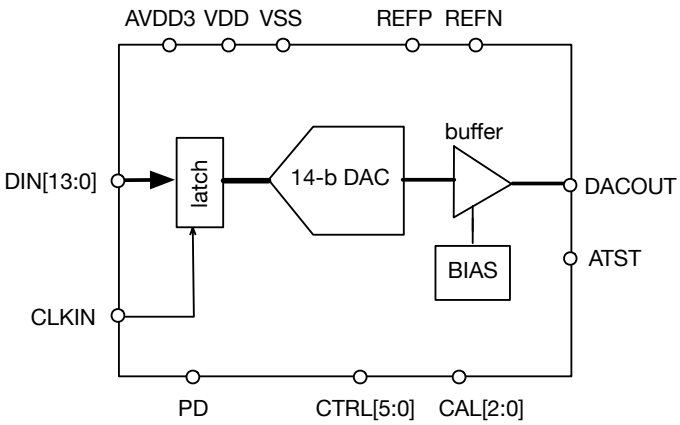

Figure 1. BLOCK DIAGRAM

APPLICATIONS

- **General purpose digital to analog converter**
- **Battery monitory system**
- **Housekeeping**
- **Auxiliary functionality**

GENERAL DESCRIPTION

IPS_GS110_DAC14_1M is compact and low power 14-bit digital-to-analog converter silicon IP. It features wide range input supply voltage from 1.7V to 5.6V. Its single-end output ranges from 0.1 to 0.9 of supply voltage.

This DAC IP is self-biased and optimized for low power and small area. At 1 MHz conversation rate, it only consumes 680uA to drive 15K/50pF loading and occupies silicon area of 0.075 mm^2.

TABLE OF CONTENTS

REVISION HISTORY

Revision	Date	Description
1.0	7/1/2016	Initial revision

DC SPECIFICATIONS FOR SUPPLY = 1.8V

T_j = 25˚C, AVDD3 = 1.8 V, VDD = 1.5V, CLKIN= 1 MHz, REFP=AVDD3, Rload= 15K ohms , unless otherwise noted.

Table 1. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		14		bits
Differential Nonlinearity (DNL) (1)		B		±2		LSB
Integral Nonlinearity (INL) (1)		B		±20		LSB
Output Voltage Range		B	0.1*AVDD3		0.9*AVDD3	V
Output Load Capacitance		B			50	pF
Output Load Resistance		B	15K			ohms
Output Noise (10Hz to 100K Hz)		B		350		uV
Offset Error		B	-1	+1	+2	% FS
Gain Error(1)		B	-10	-5	-3	% FS
Operating Junction Temperature (Tj)		B(2)	-40		125	˚C
Analog Supply Voltage AVDD3		B	1.7	1.8	2.0	V
Digital Supply Voltage VDD		B	1.35	1.5	1.65	V
AVDD3 Supply Current		B		350	620	uA
VDD Supply Current		B		2	2	uA
Power Dissipation		B		0.6	1.3	mW
Power Down Current		B		8	730	nA

(1) Measured output range from 0.1*AVDD3 to 0.9*AVDD3

(2) Measurement temperature 0~85C

Test Categories

A. Preliminary target specification.

B. Simulation of the design over process, voltage, and temperature (PVT)(1).

C. Measurements on a set of samples at typical process over voltage and temperature.

D. Measurements on a set of samples at process corners over voltage and temperature.

DC SPECIFICATIONS FOR SUPPLY = 3.3V

T_j = 25˚C, AVDD3 = 3.3 V, VDD = 1.5V, CLKIN= 1 MHz, REFP=AVDD3, Rload= 15K ohms , unless otherwise noted.

Table 2. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		14		bits
Differential Nonlinearity (DNL) (1)		B		±2		LSB
Integral Nonlinearity (INL) (1)		B		±16		LSB
Output Voltage Range		B	0.1*AVDD3		0.9*AVDD3	V
Output Load Capacitance		B			50	pF
Output Load Resistance		B	15K			ohms
Output Noise (10Hz to 100K Hz)		B		250		uV
Offset Error		B	-1	+1	+2	% FS
Gain Error(1)		B	-4	-2	-1	% FS
Operating Junction Temperature (Tj)		B(2)	-40		125	˚C
Analog Supply Voltage AVDD3		B	3.0	3.3	3.6	V
Digital Supply Voltage VDD		B	1.35	1.5	1.65	V
AVDD3 Supply Current		B		680	1100	uA
VDD Supply Current		B		2	2	uA
Power Dissipation		B		2.3	4	mW
Power Down Current		B		12	1000	nA

(1) Measured output range from 0.1*AVDD3 to 0.9*AVDD3

(2) Measurement temperature 0~85C

Test Categories

A. Preliminary target specification.

B. Simulation of the design over process, voltage, and temperature (PVT)(1).

C. Measurements on a set of samples at typical process over voltage and temperature.

D. Measurements on a set of samples at process corners over voltage and temperature.

DC SPECIFICATIONS FOR SUPPLY = 5V

T_j = 25˚C, AVDD3 = 5.0 V, VDD = 1.5V, CLKIN= 1 MHz, REFP=AVDD3, Rload= 15K ohms , unless otherwise noted.

Table 3. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		14		bits
Differential Nonlinearity (DNL) (1)		B		±2		LSB
Integral Nonlinearity (INL) (1)		B		±16		LSB
Output Voltage Range		B	0.1*AVDD3		0.9*AVDD3	V
Output Load Capacitance		B			50	pF
Output Load Resistance		B	15K			ohms
Output Noise (10Hz to 100K Hz)		B		250		uV
Offset Error		B	-1	+1	+2	% FS
Gain Error(1)		B	-1	+1	+2	% FS
Operating Junction Temperature (Tj)		B(2)	-40		125	˚C
Analog Supply Voltage AVDD3		B	4.5	5.0	5.6	V
Digital Supply Voltage VDD		B	1.35	1.5	1.65	V
AVDD3 Supply Current		B		1420	2700	uA
VDD Supply Current		B		2	2	uA
Power Dissipation		B		7	15	mW
Power Down Current		B		20	1700	nA

(1) Measured output range from 0.1*AVDD3 to 0.9*AVDD3

(2) Measurement temperature 0~85C

Test Categories

A. Preliminary target specification.

B. Simulation of the design over process, voltage, and temperature (PVT)(1).

C. Measurements on a set of samples at typical process over voltage and temperature.

D. Measurements on a set of samples at process corners over voltage and temperature.

AC SPECIFICATIONS

T_j = 25˚C, AVDD3 = 3.3 V, VDD = 1.5V, CLKIN= 1 MHz, Rload= 15K ohms, Input signal amplitude is 0.65*AVDD3, Input frequency is 150 KHz. REFP=AVDD3, unless otherwise noted.

Table 4. AC Performance

Parameter	Test conditions	Test	Min	Typ	Max	Unit
Maximum Conversion Rate		B		1		MHz
Signal-to-Noise Ratio (SNR)		B		61		dBFS
Spurious Free Dynamic Range (SFDR)		B		51		dBc
Total Harmonic Distortion (THD)		B		-50		dBc
Signal-toNoise Distortion (SNDR)		B		50		dBFS
ENOB		B		8		Bits

Note: The DAC maximum conversion rate is the time required for full scale step input and resolve to 1LSB accuracy

Note: The DAC linearity gets worse when the output gets close to VSS or AVDD3 as illustrated on Fig. 2. This is due to the output device of buffer is pushed out of saturation region and enter into the linear operation region. User can operate the DAC at the middle region to obtain good linearity.

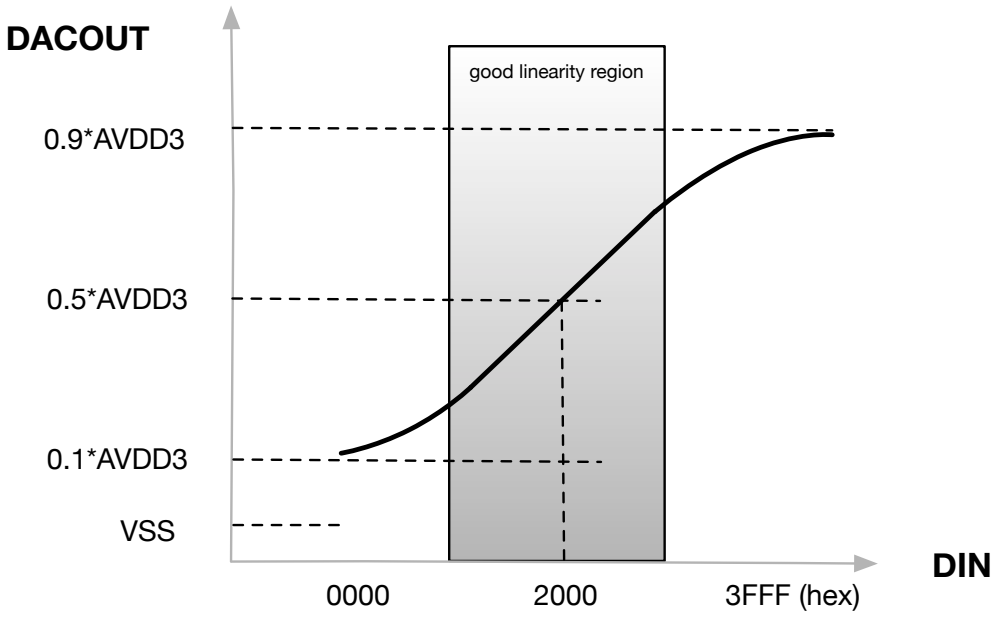

Figure 2. DAC linearity with respect to output voltage

DIGITAL SPECIFICATIONS

Table 5. Switching Specifications

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Clock Duty Cycles		A	45		55	%
Aperture Delay		A		0.5		ns
Aperture Jitter		A		<30		ps rms

PIN DESCRIPTION

Table 6. Pin Function Descriptions

Index	Pin Name	I/O	Description
1	AVDD3	AP	Analog power supply 1.9V to 5.6V
2	VDD	DP	Digital power supply 1.5V
3	VSS	DG	DAC ground
4	REFP	AI	Positive reference voltage connecting to AVDD3
5	REFN	AI	Negative reference voltage connecting to VSS
6	DIN[13:0]	DI	Digital inputs
7	CLKIN	DI	Clock input up to 1MHz
8	DACOUT	AO	Single end DAC output voltage
9	PD	DI	DAC power down control (logic 0 → power up, logic 1 → power down)
10	CTRL[5:0]	DI	Internal current and speed control bits
11	CAL[2:0]	DI	Cap mismatch calibration control bits
12	ATST	AO	Analog test output

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

TIMING DIAGRAM

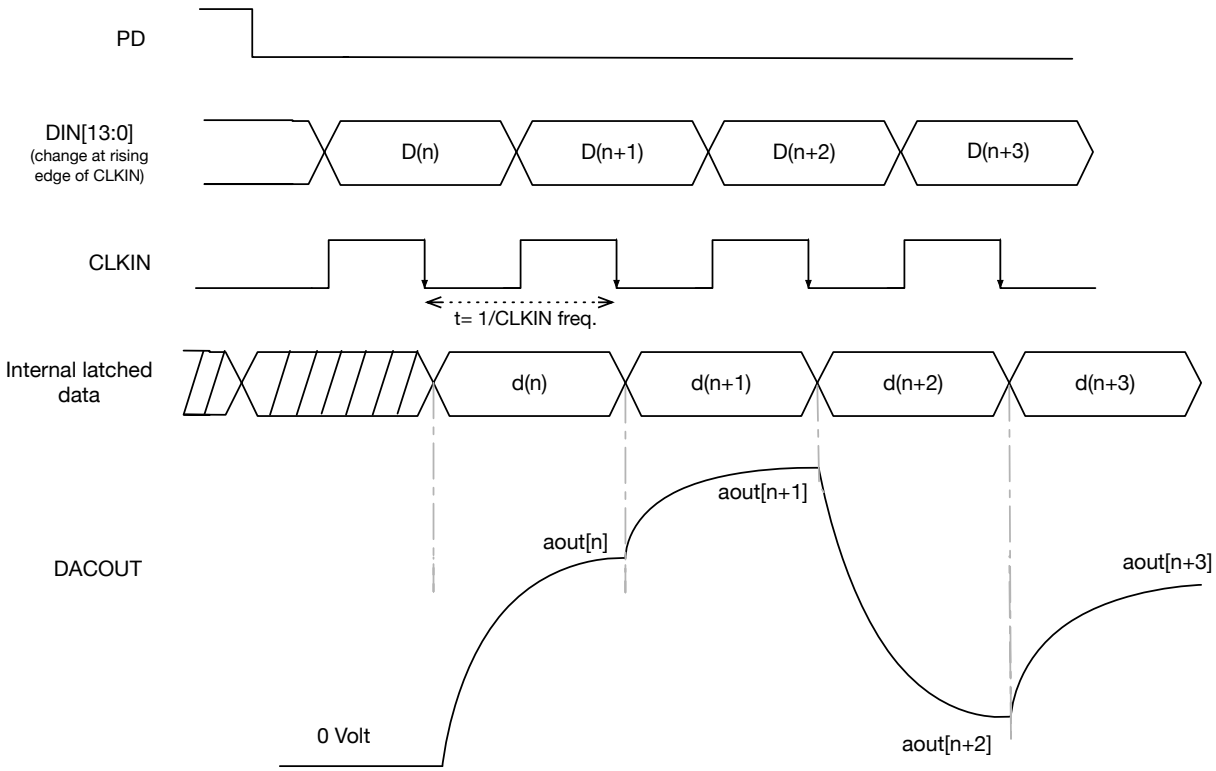

Figure 3. Timing diagram of DAC Samples

Note: DIN[13:0] should change on the rising edge of CLKIN and latched on the falling edge of CLKIN

CODE REPRESENTATION

Table 7. Binary Code Representation

DIN[13:0], Binary	Hex	Decimal	Analog output
11-1111-1111-1111	3FFF	16383	0.9*VREFP
10-0000-0000-0000	2000	8192	(VREFP+VREFN)/2
00-0000-0000-0000	0000	0	0.1*VREFP

Note: buffer is saturated to ~ 0.9*VREFP at the max. code 3FFF and is saturated to ~ 0.1*VREFP at the min. code 0000

OFFSET CALIBRATION

Table 8. DAC Calibration

CAL[2:0]	DAC bit 6	DAC bit 5
111	-8 LSB	-4 LSB
110	-12 LSB	0 LSB
101	-8 LSB	0 LSB
100	-4 LSB	0 LSB
011	+8 LSB	+4 LSB
010	+8 LSB	0 LSB
001	+4 LSB	0 LSB
000	0 LSB	0 LSB

CONTROL BITS DESCRIPTION

Table 9. Supply Control

CTRL[1:0]	Description
1 1	NOT USED
1 0	Used for AVDD3 = 5.0 V
0 1	Used for AVDD3 = 3.3 V
0 0	Used for AVDD3 = 1.8 V

Table 10. Resistive Loading Control

CTRL[3:2]	Description
1 1	NOT USED
1 0	Optimized for loading 15K
0 1	Optimized for loading 75K
0 0	Optimized for loading 500K

Note: These Supply and Loading settings should be applied to get the optimal performance

Table 11. Bias Control

CTRL[4]	Description
1	Use internal bias
0 (default)	Use external bias

Note: Internal bias will consume extra 60uA at AVDD3=3.3V

Table 12. ATST Enable Control

CTRL[5]	Description
1	ATST enabled
0 (default)	ATST disable

PHYSICAL DESCRIPTION

IP Macro Layout

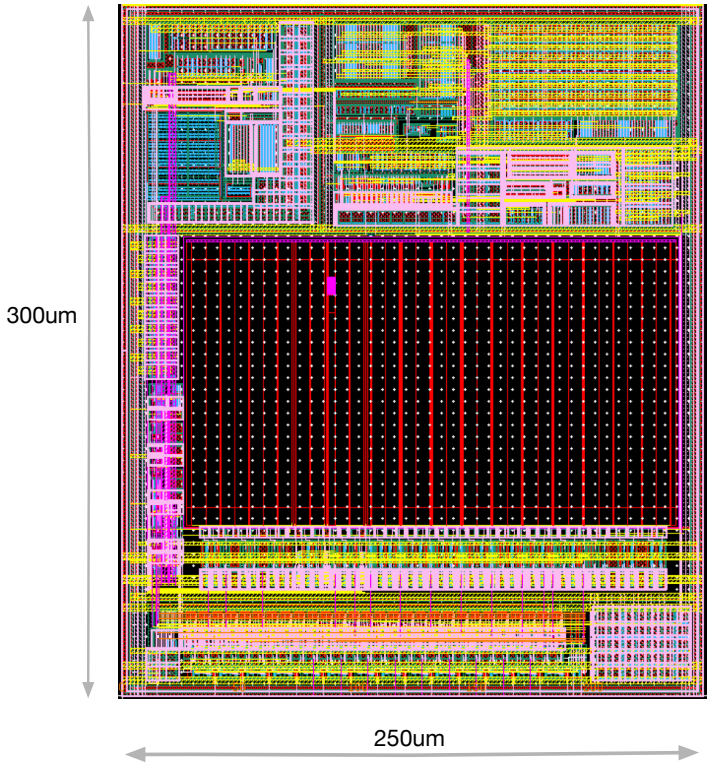

Fig. 4. IP macro layout.

DEFINITION OF SPECIFICATIONS

Offset Error

For a given gain setting, an AFE/ADC ideally produces mid-code at the output when differential input is zero. The input voltage that produces mid-code at the output is defined as the offset error.

Gain Error

AFE/ADC gain error is defined as the difference between ideal and actual full-scale values on input-output characteristics for a given gain setting when the offset error has been reduced to zero.

Integral Non Linearity (INL)

Integral non linearity of AFE/ADC transfer characteristics is defined as the deviation of the actual transfer characteristics from the ideal characteristic for a given gain setting after both offset and gain errors have been compensated. Ideal characteristic is defined as the straight line that is the best-fit of converter's transfer response.

Differential Non Linearity (DNL)

Differential non linearity of AFE/ADC transfer characteristics is defined as the deviation of analog step size from ideal step size of one LSB for a given gain setting.

ADC Latency

AFE/ADC latency (t_{pd}) is defined as the number of clock cycles between sampling edge of the clock and the clock edge at which corresponding digital outputs become available.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio is defined as the ratio of signal power to total power of all spectral components excluding DC and first eight harmonics.

Signal-to-Noise and Distortion Ratio (SNDR)

Signal-to-noise and distortion ratio is defined as the ratio of signal power to total power of all spectral components excluding DC.

Effective Number of Bits (ENOB)

Effective number of bits represents the effective resolution of the AFE. ENOB is calculated from SNDR as follows:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

Total harmonic distortion is defined as the ratio of total power of first eight harmonics to the power of fundamental signal.

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range is the difference of amplitudes in dB between signal and the highest spectral component. The highest spectral component may or may not be a harmonic.

EFFECTS OF CLOCK JITTER

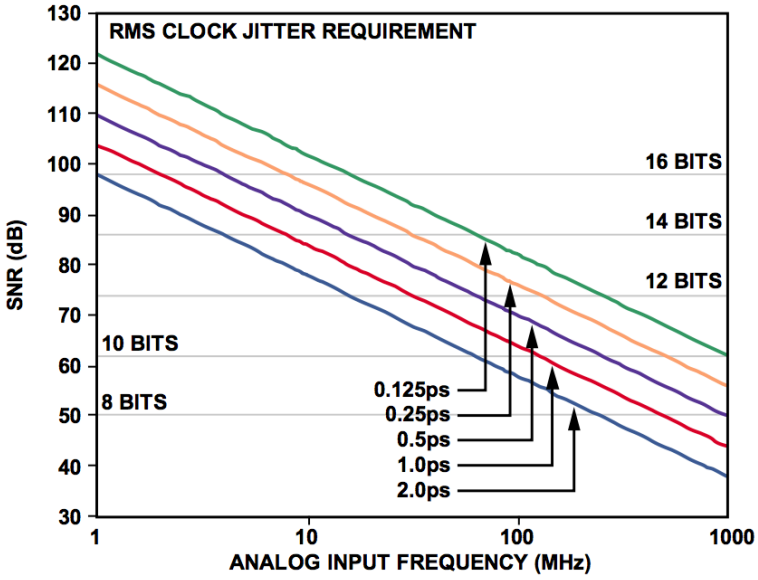

Fig. 5 Ideal SNR vs. Input Frequency and Jitter

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 13. Process Options

Item	Description
Process	GSMC 110nm Low Leakage
Metal Stack	Dual gate 5M, top metal 10.5K
MOS	NCH_ULL, PCH_ULL, NCHH_WO1, PCHH_WO1
Capacitor	MOMCAP
Resistor	RPPOLY
Deep Nwell	No
IO PAD	-

DELIVERABLES

IPSmart provides a complete design kit for fast and reliable integration of the IP into customer's design flow. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support