IPSmart

14-Bit 3 MSPS ADC in GSMC110nm

IPS_GS110_ADC14_3M

FEATURES

- **Wide Supply Range 1.7 V to 5.6V**
- **14bit, up to 3 MSPS Conversion Rate**
- **Low Power Consumption**
  150 uA @ 3 MSPS
- **Dynamic Performance @ 3MSPS**
  72 dBFS SNR
  -72 dBc THD
  74 dBc SFDR
  ENOB of 11.2
- **20 single-ended inputs or 10 differential inputs**
- **Internal reference option**
- **Ultra Small Core Area: 0.32 mm^2**
- **GSMC 110nm 1P5M**

APPLICATIONS

- **General purpose data acquisition**
- **Battery monitory system**
- **Temperature monitory system**

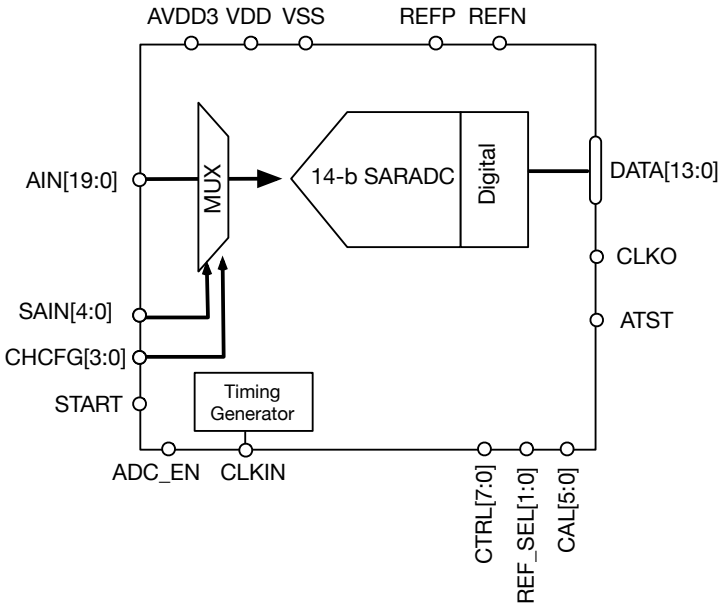

Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

IPS_GS110_ADC14_3M is compact and low power 14-bit analog-to-digital converter silicon IP. It has 20 single-end input channel selection multiplexer or 10 differential input channels selection. This ADC uses fully differential SAR architecture optimized for low power and small area. The ADC is designed for high dynamic performance for input frequencies up to Nyquist rate. This ADC consumes 150 uA at 3 MSPS operation and occupies silicon area of 0.32 mm^2. The ADC has high immunity to substrate noise and is ideal for SoC integration.

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REVISION HISTORY

Revision	Date	Description
1.0	6/1/2016	Initial revision

DC/AC SPECIFICATIONS

T_j = 25˚C, AVDD3 = 3.3 V, VDD = 1.5V, f_{IN} = 100 KHz, f_S= 3 MHz, A_{IN} = -1 dBFS, REFP= AVDD3, differential mode, unless otherwise noted.

Table 1. DC Performance

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Resolution		B		14		bits
Differential Nonlinearity (DNL)		B		±4		LSB
Integral Nonlinearity (INL)		B		±8		LSB
Input Common-Mode Voltage		B		1.65		V
Input Differential Voltage Range		B		2*AVDD3		Vpp
Input Capacitance	single-ended	B		4		pF
Absolute Gain Accuracy		B		±2		% FS
Offset Error		B		±12		LSB
Internal Voltage Reference	programmable	B	2	3	4	V
Operating Junction Temperature (Tj)		A(1)	-40		125	˚C
Analog Supply Voltage AVDD3		B	1.7	3.3	5.6	V
Digital Supply Voltage VDD		B	1.35	1.5	1.65	V
AVDD3 Supply Current		B	60	125	270	uA
VDD Supply Current		B	20	25	30	uA
Power Dissipation		B	113	450	1560	uW
Power Down Current		B	0.2	0.3	16	uA

(1) Measurement temperature 0~85C

Table 2. AC Performance

Parameter	Test conditions	Test	Min	Typ	Max	Unit
Maximum Conversion Rate		B		3		MHz
Analog Input Bandwidth		B		50		MHz
Signal-to-Noise Ratio (SNR)		B	69	72		dBFS
Spurious Free Dynamic Range (SFDR)		B	71	74		dBc
Total Harmonic Distortion (THD)		B	68	-72		dBc
Signal-toNoise Distortion (SNDR)		B	65	69		dBFS
ENOB		B	10.5	11.2		Bits

Test Categories

A. Preliminary target specification.
B. Simulation of the design over process, voltage, and temperature (PVT)[1].
C. Measurements on a set of samples at typical process over voltage and temperature.
D. Measurements on a set of samples at process corners over voltage and temperature.

DIGITAL SPECIFICATIONS

Table 3. Switching Specifications

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Clock Duty Cycles		A	45		55	%
Aperture Delay		A		0.5		ns
Aperture Jitter		A		<30		ps rms

PIN DESCRIPTION

Table 4. Pin Function Descriptions

Index	Pin Name	I/O	Description
1	AVDD3	AP	Analog power supply 1.7V to 5.6V, default is 3.3V
2	VDD	DP	Digital power supply 1.5V
3	VSS	DG	ADC ground
4	REFP	AI	Positive reference voltage connecting to AVDD3
5	REFN	AI	Negative reference voltage connecting to VSS
6	CLKIN	DI	Input clock, note that input clock frequency is the sampling rate
7	AIN[19:0]	AI	Analog inputs channels
8	CHCFG[3:0]	DI	Channel configuration control bits
9	SAIN[4:0]	DI	Input channel select bits
10	REF_SEL[1:0]	DI	Internal reference voltage selection (2V, 3V or 4V)
11	START	DI	Start of conversion
12	ADC_EN	DI	ADC enable control input (logic 1 → power up, logic 0 → power down)
13	CLKO	DO	Output clock, can be used to sample DATA[13:0]
14	DATA[13:0]	DO	14-bit output data of ADC
15	CTRL[7:0]	DI	Internal reference and speed control bits
16	CAL[5:0]	DI	Cap mismatch calibration control bits
17	ATST	AO	Analog test output

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

INPUT CHANNEL SELECTION

The input channels can be configured as:

(1) Single ended mode – 20 channels or

(2) Differential mode – 8 differential pair and 4 single ended channels

Single and Differential inputs are configured via Channel Configuration (CHCFG) signal:

Table 5. Differential/Single end Channel Configuration

CHCFG [3:0]	Channel Configuration	Description
0000	0 differential pair, 16 single ended inputs	Differential pair: None Single ended: AIN0 to AIN15
0001	1 differential pair, 14 single ended inputs	Differential pair: AIN14/AIN15 Single ended: AIN0 to AIN13
0010	2 differential pair, 12 single ended inputs	Differential pair: AIN12/AIN13, AIN14/AIN15 Single ended: AIN0 to AIN11
0011	3 differential pair, 10 single ended inputs	Differential pair: AIN10/AIN11, AIN12/AIN13, AIN14/AIN15 Single ended: AIN0 to AIN9
0100	4 differential pair, 8 single ended inputs	Differential pair: AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, AIN14/AIN15 Single ended: AIN0 to AIN7
0101	5 differential pair, 6 single ended inputs	Differential pair: AIN6/AIN7, AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, AIN14/AIN15 Single ended: AIN0 to AIN5
0110	6 differential pair, 4 single ended inputs	Differential pair: AIN4/AIN5, AIN6/AIN7, AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, AIN14/AIN15 Single ended: AIN0 to AIN3
0111	7 differential pair, 2 single ended inputs	Differential pair: AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, AIN14/AIN15 Single ended: AIN0 to AIN1
1000	8 differential pair, 0 single ended inputs	Differential pair: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, AIN14/AIN15 Single ended: None
Other	Reserved	

When CHCFB[3:0] are configured as single end mode, analog input channels are selected via the Analog Input Channel Select (SAIN) signal:

Table 6. Single end Inputs Channel Selection

SAIN	Analog Input Channel Select	SAIN	Analog Input Channel Select
00000	AIN0	01010	AIN10
00001	AIN1	01011	AIN11
00010	AIN2	01100	AIN12
00011	AIN3	01101	AIN13
00100	AIN4	01110	AIN14
00101	AIN5	01111	AIN15
00110	AIN6	10000	AIN16
00111	AIN7	10001	AIN17
01000	AIN8	10010	AIN18
01001	AIN9	10011	AIN19
		10100 ~ 11111	ADC OFFSET calibration

Note: Channel # 16 to 19 are for internal use and are always single ended. They are always available regardless of number of differential pair selected.

When CHCFB[3:0] are configured as differential mode, analog input channels are selected via the Analog Input Channel Select (SAIN) signal:

Table 7. Differential Inputs Channel Selection

SAIN	Analog Input Channel Select	SAIN	Analog Input Channel Select
00000	AIN0/AIN1	01000	AIN8/AIN9
00010	AIN2/AIN3	01010	AIN10/AIN11
00100	AIN4/AIN5	01100	AIN12/AIN13
00110	AIN6/AIN7	01110	AIN14/AIN15

TIMING DIAGRAM

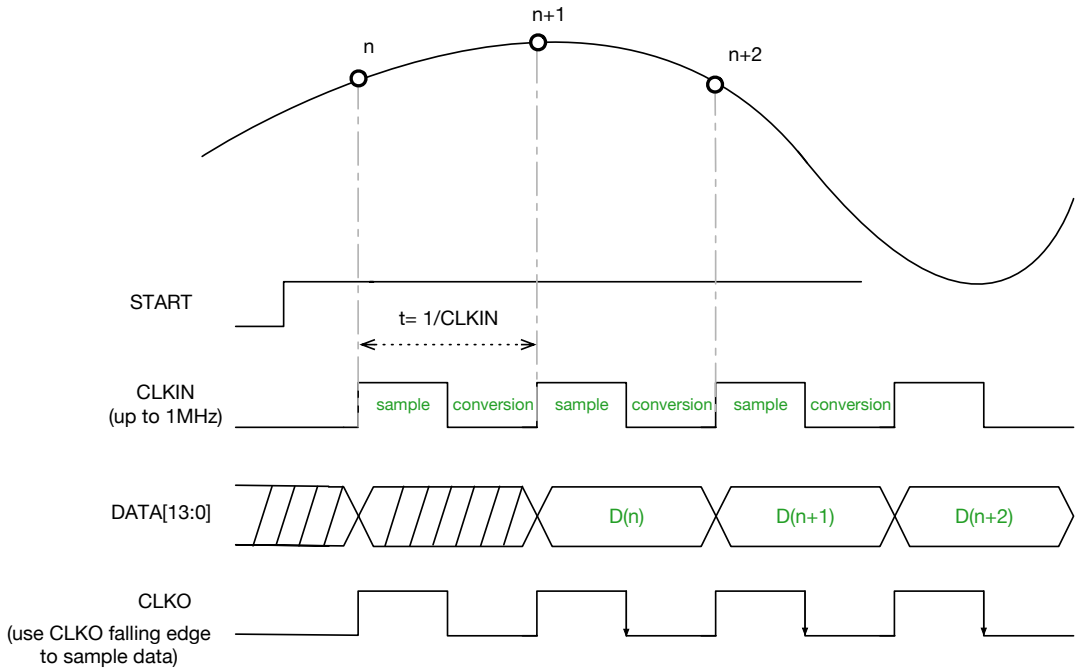

Figure 2. ADC Timing Diagram of continuous samples

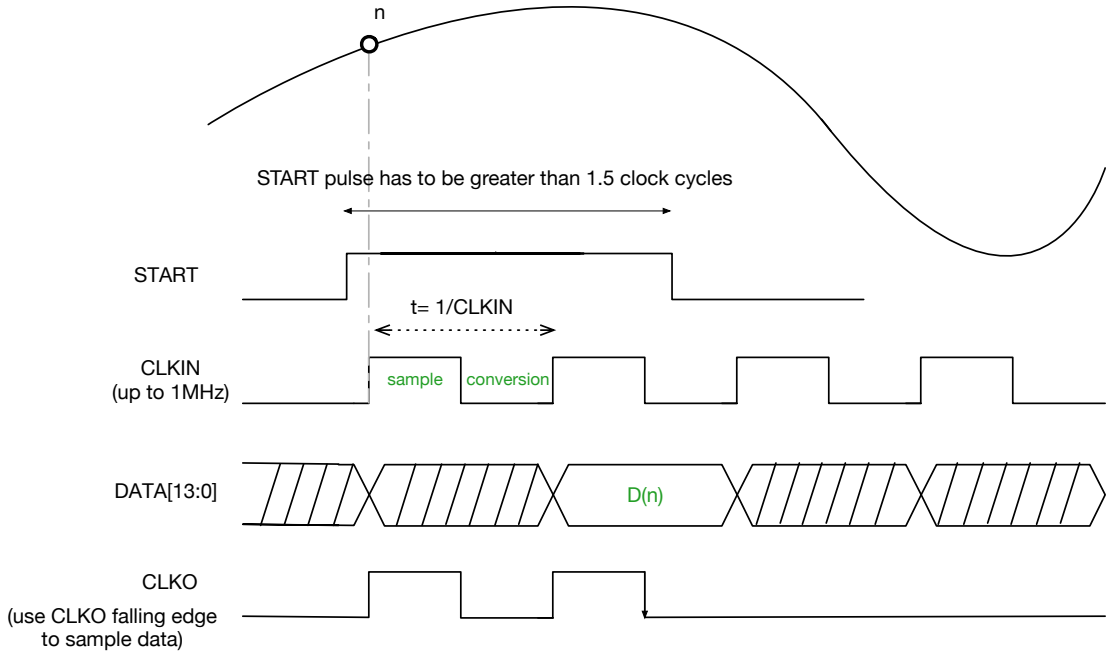

Figure 3. ADC Timing Diagram of single conversion

CODE REPRESENTATION

Table 8. Code Description for 2's complement when CTRL[4]= 1

Analog Input (INP-INN)	Hex	Decimal	DO[13:0] 2's Complement
REFP	1FFF	+8191	01-1111-1111-1111
0	0000	0	00-0000-0000-0000
-REFP	2000	-8192	10-0000-0000-0000

Table 9. Code Description for Binary when CTRL[4]= 0

Analog Input INP	Hex	Decimal	DO[13:0], Binary
REFP	3FFF	16383	11-1111-1111-1111
REFP/2	2000	8192	10-0000-0000-0000
0	0000	0	00-0000-0000-0000

Note: Code representation is programmable through CTRL[4]

CONTROL BITS DESCRIPTION

Table 10. ATST Control

CTRL[7]	Description
1	ATST enable
0	ATST disable

Note: when CTRL[7] is asserted, internal VCM voltage can be measured on ATST pin with REF_SEL[1:0] setting = 00; internal REFP voltage can be measured on ATST pin with REF_SEL[1:0]= 11, 10 or 01.

Table 11. VCM_GEN Buffer Control

CTRL[6]	Description
1	VCM_GEN extra buffer enable
0	VCM_GEN extra buffer disable

Table 12. LSB Average Control

CTRL[5]	Description
1	LSB averaging enable
0	LSB averaging disable

Table 13. Code Representation Control

CTRL[4]	Description
1	2’s complement
0	Unsigned binary

Table 14. SAR Timing 1 Delay Control

CTRL[3:2]	Description	Remarks
11	50ns	For AVDD3= 1.8V
10	30ns	For AVDD= 3V
01	10ns	For AVDD= 3V
00	5ns	For AVDD= 5.6V

Table 15. SAR Timing 2 Delay Control

CTRL[1:0]	Description	Remarks
11	95ns	For AVDD3= 1.8V
10	15ns	For AVDD= 3V
01	10ns	For AVDD= 3V
00	5ns	For AVDD= 5.6V

Table 16. ADC Reference Control

REF_SEL[1:0]	Description	Remarks
11	4.0V	ATST=REFP
10	3.0V	ATST=REFP
01	2.0V	ATST=REFP
00	External REF	ATST= VCM

OFFSET CALIBRATION

Table 17. Capacitive DAC N side

CAL[5:3]	N CDAC[6]	N CDAC[5]
111	-8 LSB	-4 LSB
110	-12 LSB	0 LSB
101	-8 LSB	0 LSB
100	-4 LSB	0 LSB
011	+8 LSB	+4 LSB
010	+8 LSB	0 LSB
001	+4 LSB	0 LSB
000	0 LSB	0 LSB

Table 18. Capacitive DAC P side

CAL[2:0]	P CDAC[6]	P CDAC[5]
111	-8 LSB	-4 LSB
110	-12 LSB	0 LSB
101	-8 LSB	0 LSB
100	-4 LSB	0 LSB
011	+8 LSB	+4 LSB
010	+8 LSB	0 LSB
001	+4 LSB	0 LSB
000	0 LSB	0 LSB

Note: CAL[2:0] control P side DAC and CAL[5:3] control N side DAC

PHYSICAL DESCRIPTION

IP Macro Layout: 620 um X 520 um

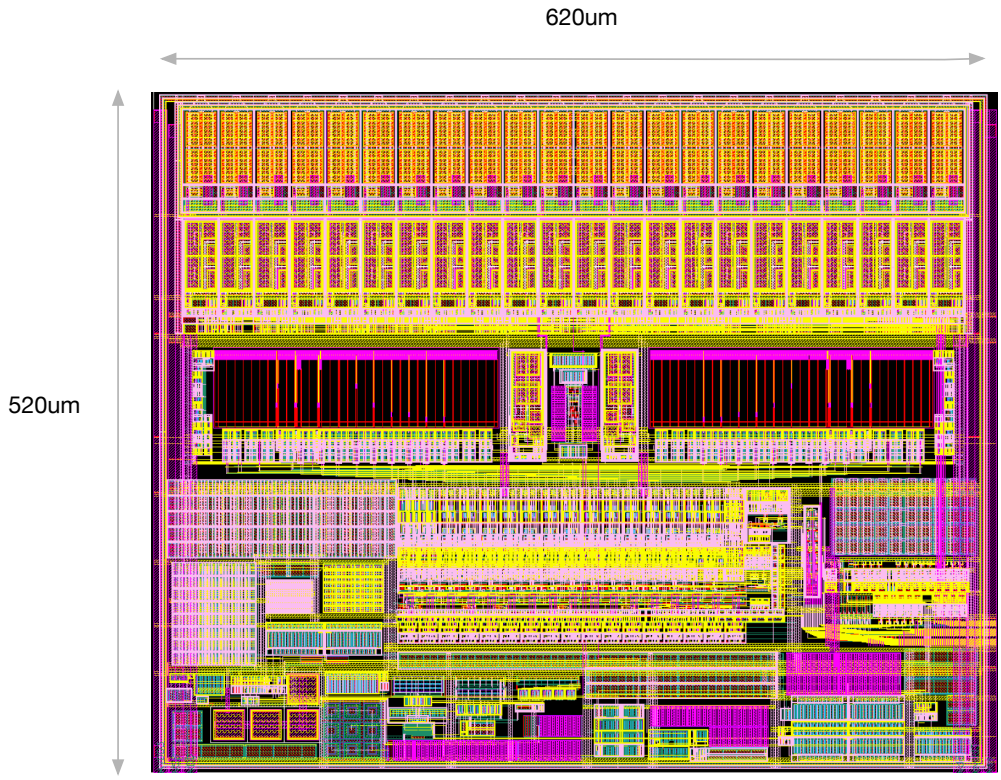

Fig. 4. IP macro layout.

DEFINITION OF SPECIFICATIONS

Offset Error

For a given gain setting, an AFE/ADC ideally produces mid-code at the output when differential input is zero. The input voltage that produces mid-code at the output is defined as the offset error.

Gain Error

AFE/ADC gain error is defined as the difference between ideal and actual full-scale values on input-output characteristics for a given gain setting when the offset error has been reduced to zero.

Integral Non Linearity (INL)

Integral non linearity of AFE/ADC transfer characteristics is defined as the deviation of the actual transfer characteristics from the ideal characteristic for a given gain setting after both offset and gain errors have been compensated. Ideal characteristic is defined as the straight line that is the best-fit of converter's transfer response.

Differential Non Linearity (DNL)

Differential non linearity of AFE/ADC transfer characteristics is defined as the deviation of analog step size from ideal step size of one LSB for a given gain setting.

ADC Latency

AFE/ADC latency (t_{pd}) is defined as the number of clock cycles between sampling edge of the clock and the clock edge at which corresponding digital outputs become available.

Signal-to-Noise Ratio (SNR)

Signal-to-noise ratio is defined as the ratio of signal power to total power of all spectral components excluding DC and first eight harmonics.

Signal-to-Noise and Distortion Ratio (SNDR)

Signal-to-noise and distortion ratio is defined as the ratio of signal power to total power of all spectral components excluding DC.

Effective Number of Bits (ENOB)

Effective number of bits represents the effective resolution of the AFE. ENOB is calculated from SNDR as follows:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

Total harmonic distortion is defined as the ratio of total power of first eight harmonics to the power of fundamental signal.

Spurious-Free Dynamic Range (SFDR)

Spurious-free dynamic range is the difference of amplitudes in dB between signal and the highest spectral component. The highest spectral component may or may not be a harmonic.

EFFECTS OF CLOCK JITTER

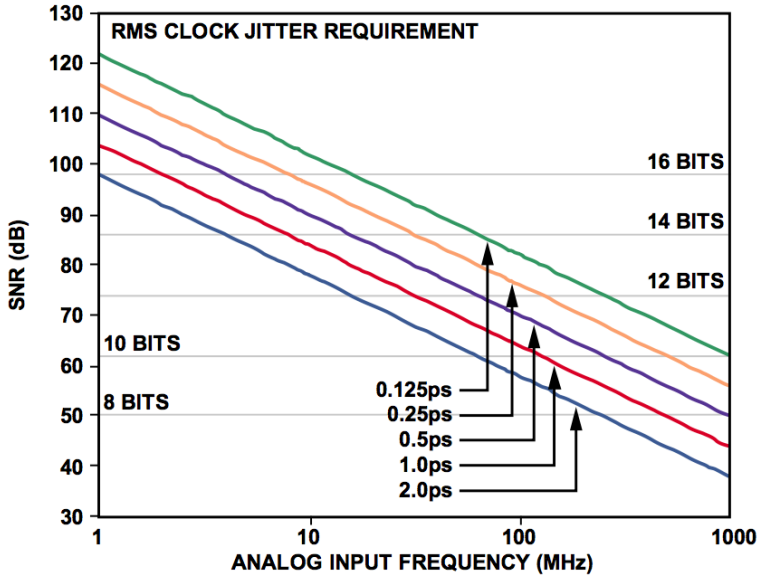

Fig. 5 Ideal SNR vs. Input Frequency and Jitter

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 19. Process Options

Item	Description
Process	GSMC 110nm Low Leakage
Metal Stack	Dual gate 5M, top metal 10.5K
MOS	NCH_ULL, PCH_ULL, NCHH_WO1, PCHH_WO1
Capacitor	MOMCAP
Resistor	RPPOLY
Deep Nwell	No
IO PAD	-

DELIVERABLES

IPSmart provides a complete design kit for fast and reliable integration of the IP into customer's design flow. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support