IPSmart

12-Bit 200MSPS DAC in UMC 40LP

IPX_U40L_DAC12_200M

FEATURES

- **12-bit DAC, up to 200 MSPS**
- **Dual 3.3V / 1.1 V Supply**
- **Low Power Consumption**
  11mW @ 200 MSPS
- **Superior Dynamic Range**
  62dB SNR @ f_{out} = 46 MHz
  53dBc SFDR @ f_{out} = 46 MHz
- **IFS = 0.5/1.0/1.5/2 mA**
- **Output voltage: up to 2.6Vppd**
- **Current or voltage output option**
- **Ultra Small Core Area: 0.06 mm^2**
- **UMC 40LP 1P7M1H**

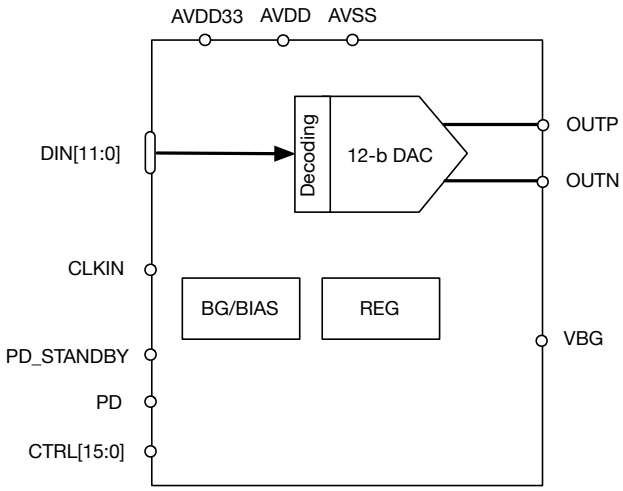


Figure 1. BLOCK DIAGRAM

APPLICATIONS

- **WiFi / LTE / WiMax**
- **Wireless MIMO**
- **Digital Video**
- **Communication Transmit**

GENERAL DESCRIPTION

IPX_U40L_DAC12_200M is compact and ultra low power 12-bit digital-to-analog converter silicon IP in UMC 40nm LP process. It features up to single end 1.3V or 2.6Vppd large output amplitude.

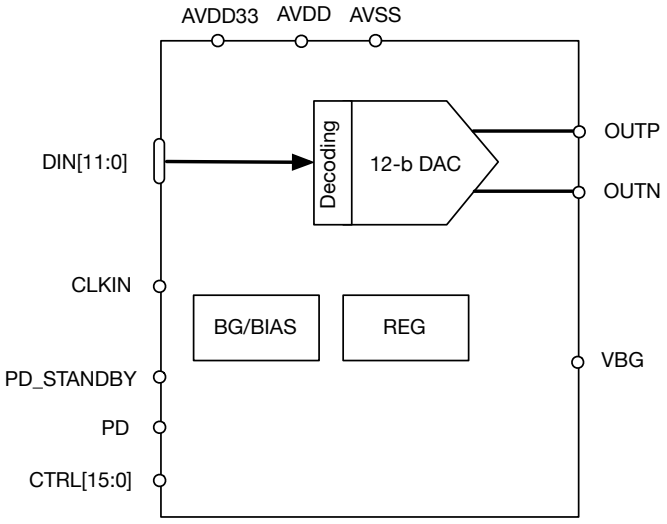
This DAC IP is optimized for low power and small area. At 200 MHz conversation rate, it only consumes 11mW and occupies silicon area 300um x 200um= 0.06 mm^2.

PIN DESCRIPTION

Table 1. Pin Function Descriptions (total 37 pins)

Index	Pin Name	I/O	Description
1	AVDD33	AP	Analog power supply 3.3V
2	AVDD	AP	Analog power supply 1.1V
3	AVSS	AG	Analog ground for AVDD33 and AVDD
4	DIN[11:0]	DI	12-bit digital inputs (unsigned binary code)
5	CLKIN	DI	Clock input
6	OUTP/OUTN	AO	Differential outputs
7	PD_STANDBY	DI	DAC standby mode, clock inside DAC is disabled
8	PD	DI	DAC power down mode, all blocks are disabled
9	CTRL[15:0]	DI	Programmable control bits, see table 8-15 for details
10	VBG	AO	Bandgap output voltage, refer to table 11

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output



CODE REPRESENTATION

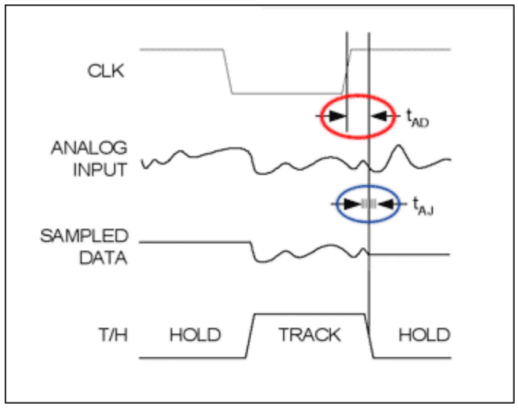
Table 2. Input Code Description (@ max 2.6Vppd)

DIN[11:0] (unsigned binary)	Hex	Decimal representation	OUTP	OUTN
1111-1111-1111	FFF	4095	1.3V	0
1000-0000-0000	800	2048	0.65V	0.65V
0000-0000-0000	000	0	0	1.3V

DIGITAL SPECIFICATIONS

Table 3. Switching Specifications

Parameter	Test Conditions	Test	Min	Typ	Max	Unit
Clock Duty Cycles		B	46		54	%
Aperture Delay (t_{AD})		B		0.2		ns
Aperture Jitter (t_{AJ})		B		<5		ps rms



Aperture delay (red) and jitter (blue).

TIMING DIAGRAM

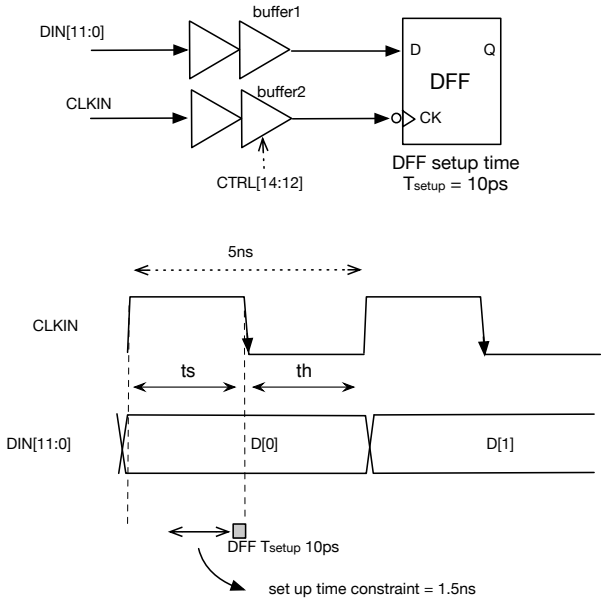


Fig. 2. DAC Input Timing Diagram

Note 1. DAC's internal DFF latches the input data on the falling edge of CLKIN

2. The DFF setup time is < 20ps
3. Setup time constraint is 1.85ns and hold time constraint is zero
4. Control register CTRL[13:12] is used to adjust the delay of falling edge CLKIN and CTRL[14] inverts the falling edge to rising edge in case there is potential timing issue

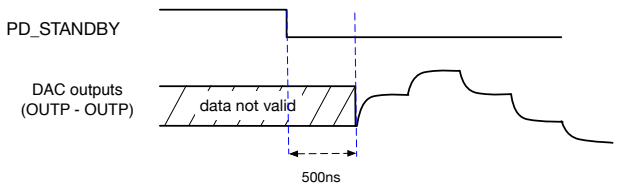


Fig. 3. Timing Diagram of Wake-Up from standby mode

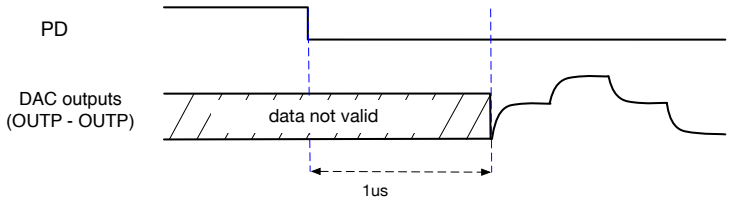


Fig. 4. Timing Diagram of Power-Up from power down mode

LOAD MODEL AND OTUPUT SWING

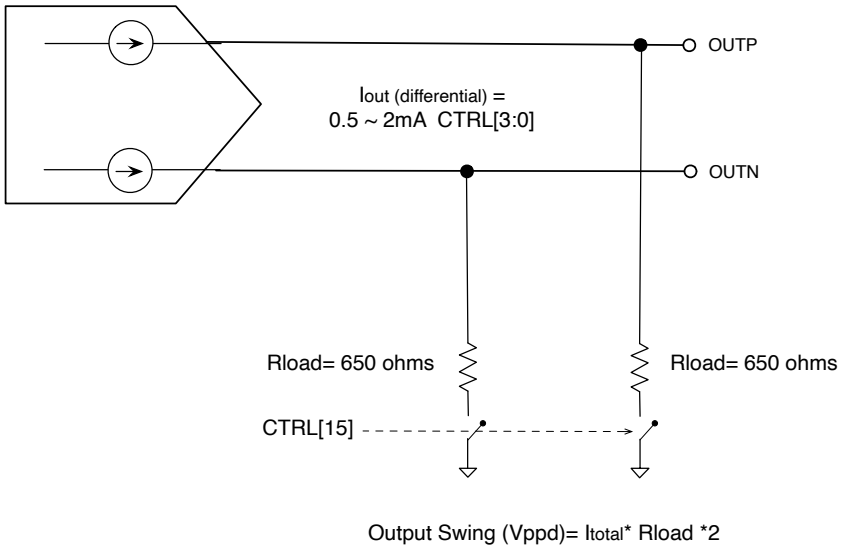


Fig. 5. DAC output load model

Table 4. DAC FS Current Control Bits

CTRL[3:0]	Decimal of CTRL[3:0]	FS Current (mA)	Single end maximum output voltage
0000	0	0.5mA	0.325V
0100	4	0.5mA+4*0.1mA= 0.9mA	0.585V
1000	8	0.5mA+8*0.1mA= 1.3mA	0.845V
...	…	…	…
1010	10	0.5mA+10*0.1mA= 1.5mA	0.98V
1011	11	0.5mA+11*0.1mA= 1.6mA	1.04V
1100	12	0.5mA+12*0.1mA= 1.7mA	1.1V
1111	15	0.5mA+15*0.1mA= 2mA	1.3V

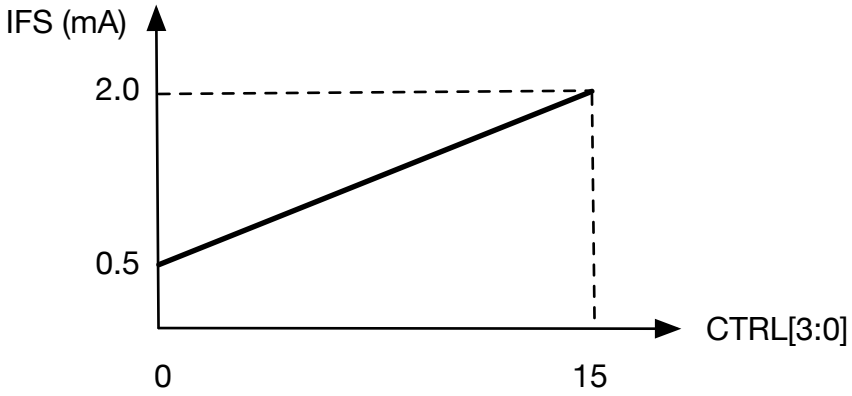


Fig. 6. DAC full scale current versus gain control bits CTRL[3:0].

The full-scale current of DAC can be adjusted by 4-bit control bit CTRL[3:0]

Full scale current IFS = 0.5mA + CTRL[3:0]*0.1mA

OUTP/OUTN (max) = IFS*650 ohms= 0.325 + CTRL[3:0]*65mV

CONTROL BITS DESCRIPTION

Table 5. Full Scale Current Control

CTRL[3:0]	Description
1 1 1 1	2.0 mA
1 1 1 0	1.9 mA
1 1 0 1	1.8 mA
1 1 0 0	1.7 mA
1 0 1 1	1.6 mA
1 0 1 0	1.5 mA
…..	…..
0 1 0 0	0.9 mA
0 0 0 0	0.5 mA

Table 6. Internal RVDD15 Adjustment

CTRL[5:4]	Description
1 1	1.50 V
1 0 (default)	1.48 V
0 1	1.45 V
0 0	1.40 V

Table 7. Internal RVDD05 Adjustment

CTRL[7:6]	Description
1 1	0.47 V
1 0	0.44 V
0 1 (default)	0.42 V
0 0	0.40 V

Table 8. Bandgap Voltage Adjustment

CTRL[9:8]	Description
1 1	1.114 V
1 0	1.165 V
0 1	1.165 V
0 0	1.216 V

Table 9. Bandgap Temp. Coeff. Adjustment

CTRL[11:10]	Description
1 1	Positive temp. coeff. +2
1 0	Positive temp. coeff. +1
0 1 (default)	Positive temp. coeff. +0
0 0	Positive temp. coeff. -1

Table 10. Input Data Sampling Delay Control

CTRL[13:12]	Description
1 1	100ps
1 0	200ps
0 1 (default)	300ps
0 0	400ps

Table 11. Sampling Clock Edge Control

CTRL[14]	Description
1	Sample input data at the rising edge of CLKIN
0 (default)	Sample input data at the falling edge of CLKIN

Table 12. Disable Internal Resistor Load

CTRL[15]	Description
1	Use external resistor load (current output)
0 (default)	Use internal resistor load (voltage output)

PHYSICAL DESCRIPTION

IP Macro Layout

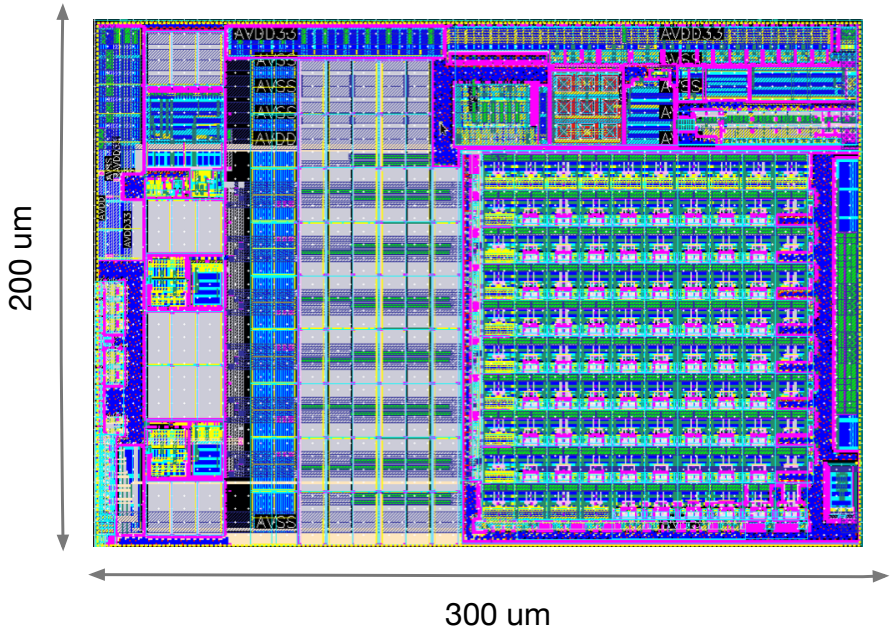


Fig. 7. Estimated IP macro layout: 300 x 200um= 0.06 mm^2

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 13. Process Options

Item	Description
Process	UMC 40nm LP
Metal Stack	1P7M0T1H0A0U RDL 14.5K
Transistors	Core RVT, 25OD33
Resistor	RNPPO_LP
Deep Nwell	Yes
IO PAD	-

DELIVERABLES

IPSmart will provide complete design kit for fast and reliable integration of the IP. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (System Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support