12-Bit 480MSPS IQ DAC in SMIC 40nm L

S40L_DAC12X2_480M

FEATURES

- **Dual 12-bit DAC, up to 480 MSPS**
- **Dual 3.3 V / 1.1 V Supply**
- **Low Power Consumption**
  185mW @ 480 MSPS
- **Superior Dynamic Range**
  68dBc SFDR @ f_{out} = 80 MHz
- **IFS = 10~20mA with programmability**
- **Output voltage: 1.6Vppd with 50 ohms loading**
- **Core Area: 1.6 mm^2**
- **SMIC 40LL 1P9M2TM**

APPLICATIONS

- **WiFi / LTE / WiMax**
- **Wireless MIMO**
- **Digital Video**
- **Communication Transmit**

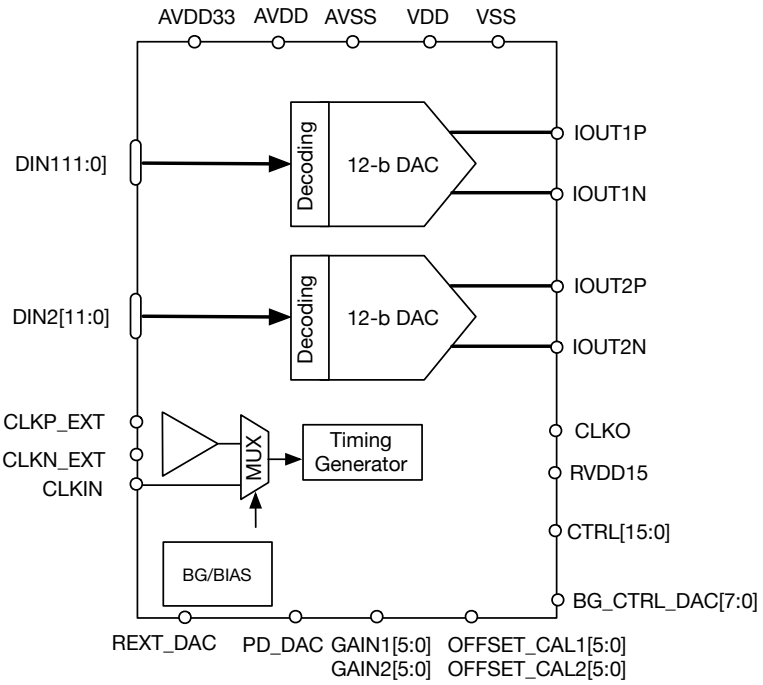

Figure 1. BLOCK DIAGRAM

GENERAL DESCRIPTION

S40L_DAC12X2_480M is compact and low power 12-bit digital-to-analog converter silicon IP in SMIC 40nm LP process. It features two channel current steering DAC.

This IQ DAC IP is optimized for low power and small area. At 480 MHz conversation rate, it consumes 185mW and occupies silicon area of 1.6 mm^2.

PIN DESCRIPTION

Table 1. Pin Function Descriptions

Index	Pin Name	I/O	Description
1	AVDD33	AP	Analog power supply 3.3V
2	AVDD	AP	Analog power supply 1.1V
3	VDD	DP	Digital power supply 1.1V
4	AVSS	AG	Analog ground
5	VSS	DG	Digital ground
6	REXT_DAC	AI	Place 25K ohms resistor and 1uF cap to gnd
7	DIN1[11:0],DIN2[11:0]	DI	Digital inputs
8	CLKIN_SOC	DI	SOC input sampling clock
9	CLKIN_EXT	DI	External input sampling clock
10	IOUT1P/IOUT1N	AO	Channel 1 differential outputs
11	IOUT2P/IOUT2N	AO	Channel 2 differential outputs
12	GAIN1[5:0], GAIN2[5:0]	DI	DAC 6-bit IFS full scale current control
13	PD_DAC	DI	DAC power down control, logic 1 → power down
14	OFFSET_CAL1[5:0], OFFSET_CAL2[5:0]	DI	DAC offset current control bits
16	CLKO	DO	Output clock (buffered CLKIN)
17	CTRL[15:0]	DI	Control registers

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

FULL SCALE CURRENT CONTROL

Table 2. DAC FS Current Control Bits

GC[5:0]	Decimal of GC[5:0]	FS Current (mA)
00-0000	0	11
…	…	…
01-0000	16	13.8
…	…	…
10-0000	32	16.6
...	…	…
11-0000	48	19.4
...	…	…
11-0100	52	20.1
...	…	…
11-1111	63	22

The full-scale current of DAC can be adjusted by 6-bit control bit GC[5:0]

$$I_{FS} = 11mA + GC[5:0]/63 * 11mA = 11mA + GC[5:0] * 0.17mA$$

$$IOUTP = Vcm + Vdiff = 0.5 * IFS * 50 + (DI - 32768)/65536 * IFS * 50$$
$$IOUTN = Vcm - Vdiff = 0.5 * IFS * 50 - (DI - 32768)/65536 * IFS * 50$$

* DI is the decimal representation of Table 4

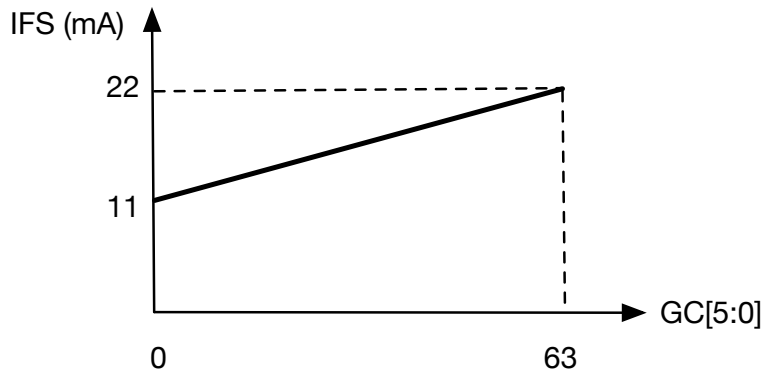

Fig. 3. DAC full scale current versus gain control bits GC[5:0].

PHYSICAL DESCRIPTION

IP Macro Layout (estimated)

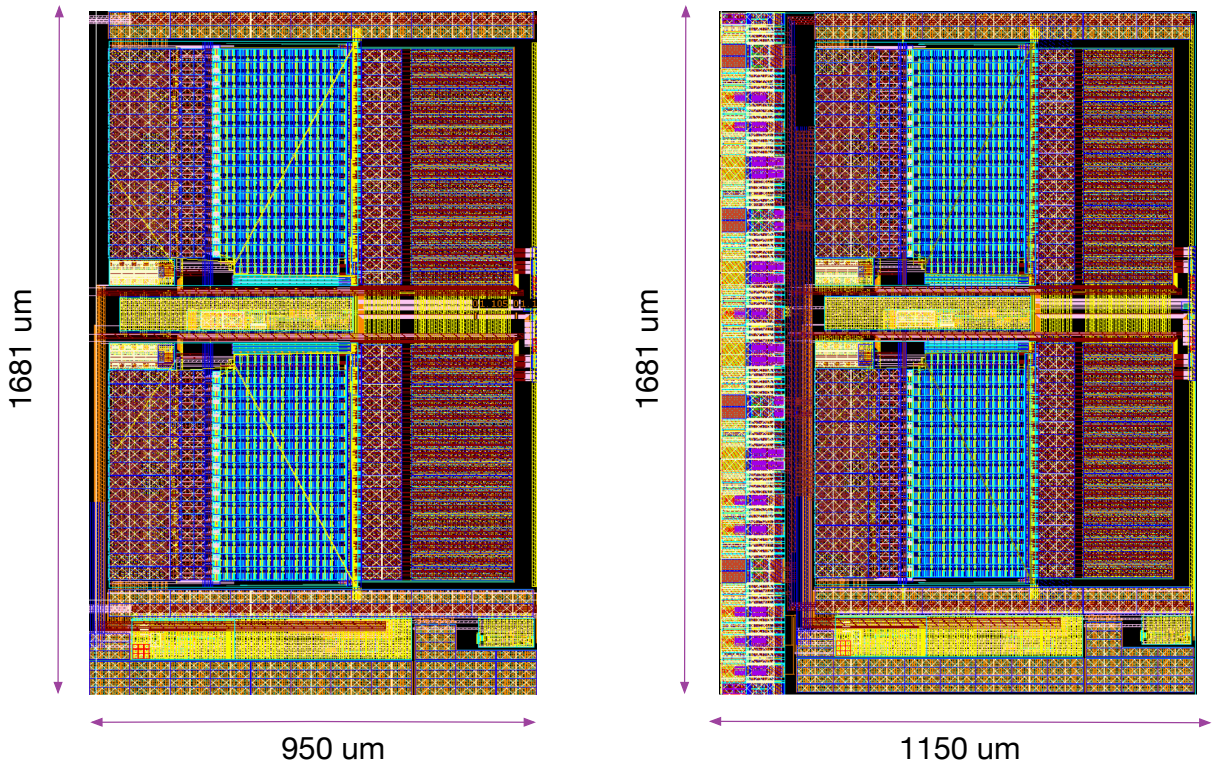

Fig. 2. IP macro layout. 950x1681um (w/o pads); 1150x1681 um (w pads)

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 3. Process Options

Item	Description
Process	SMIC 40nm LL
Metal Stack	1P9M2TM (M1~M7, M8/M9 are thick metals)
Resistor	P+ Poly
Deep Nwell	No
IO PAD	-

DELIVERABLES

Complete design kit for fast and reliable integration of the IP is provided. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (System Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support