14-Bit 125 MSPS ADC in SMIC 40L

S40L_ADC14X8_125M

FEATURES

- **Dual Supply 2.5/1.1V**
- **125 MSPS Conversion Rate**
- **Current Consumption**
  185 mW per channel @ 125 MSPS
- **Dynamic Performance @ 125 MSPS**
  68 dBFS SNR
  78 dBc SFDR
  ENOB of 11.0
- **Precision Bandgap and BIAS**
- **Programmable full scale**
- **Ultra Small Core Area: 4.7 mm X 1.2 mm= 5.6 mm^2**
- **SMIC 40LL 1P9M2TM**

APPLICATIONS

- **WiFi, HDTV, Video Application**
- **Communication RX Channel**
- **Digital Imaging**

GENERAL DESCRIPTION

S40L_ADC14X8_125M is compact and low power 14-bit analog-to-digital converter silicon IP. This 8 channel ADC IP is optimized for low power 185 mW (per channel) and small area 5.6 mm^2 (8 channel) at 125MSPS operation.

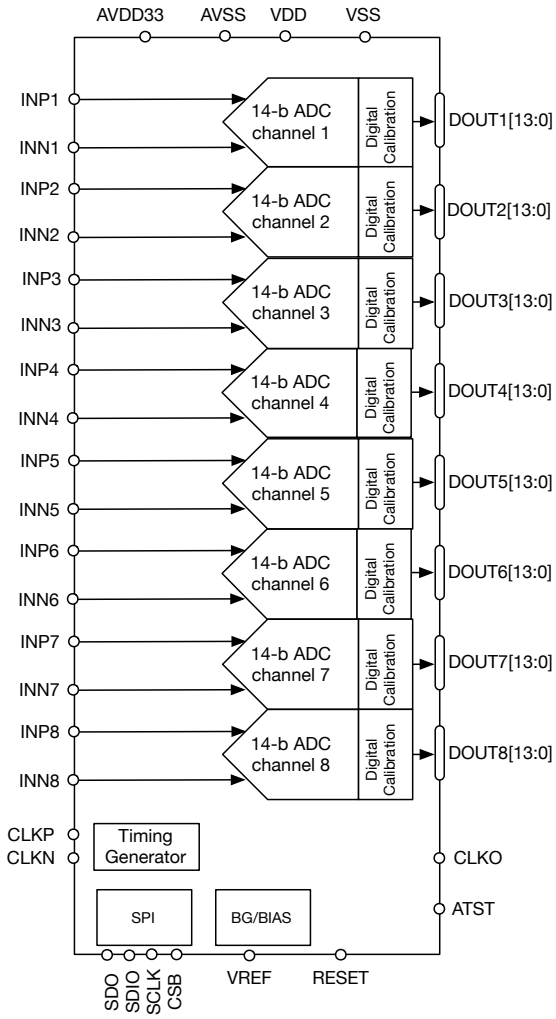

Figure 1. BLOCK DIAGRAM

The ADC has high immunity to substrate noise and is ideal for integration into SoC.

PIN DESCRIPTION

Table 1. Pin Function Descriptions

Index	Pin Name	I/O	Description
1	AVDD25	AP	Analog power supply 2.5 V
2	AVDD	AP	Analog power supply 1.1 V
3	VDD	DP	Digital power supply 1.1V
4	AVSS	AG	Analog ground
5	VSS	DG	Digital ground
6	INP1/INN1 ~ INP8/INN8	AI	8 channel analog differential inputs
7	CLKIN_SOC	DI	SOC input sampling clock
8	CLKP_EXT/ CLKN_EXT	DI	External input sampling clock
9	CLKO[7:0]	DO	Output clock used to sample DOUT[15:0]
10	DOUT1[13:0] ~ DOUT8[13:0]	DO	8 channel 14-bit output data of ADC
11	ATST	AO	Analog test point output
12	REXT_ADC	AO	Place 25K ohms resistor and 1uF cap to gnd
13	PD[7:0]	DI	ADC channel power down control, logic 1 → power down
14	CTRL1[15:0]	DI	General control registers (all 8 channels shares)
15	CTRL2[63:0]	DI	Independent channel control bits

P: Power, **G:** Ground, **A**: Analog, **D**: Digital, **I**: input, **O**: Output

PHYSICAL DESCRIPTION

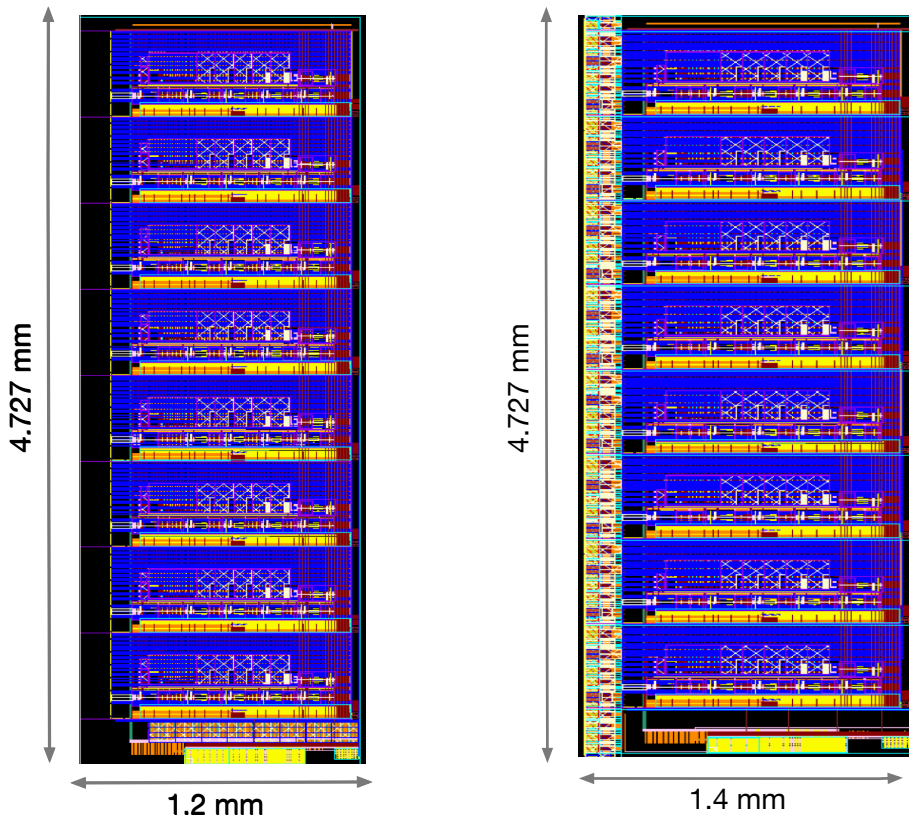

Fig. 2. IP macro layout. 1200x4727um (w/o pad), 1400x4727 (with pads)

PROCESS

The IP layout (GDSII) is available in the following process and metal stack options.

Table 18. Process Options

Item	Description
Process	SMIC 40nm LL
Metal Stack	1P9M2TM (M1~M7, M8/M9 are thick metals)
Capacitor	MOMCAP
Resistor	RPPOLY
Deep Nwell	No
IO PAD	-

DELIVERABLES

Complete design kit for fast and reliable integration of the IP is provided. The design kit includes the following:

- Full datasheet
- Physical design database (GDSII format)
- LVS netlist (SPICE compatible)
- Footprint (.LEF format)
- Behavioral model (System Verilog model)
- Timing model (.LIB format)
- Integration guidelines and support